深圳市方九电子科技有限公司

Shenzhen Fangjiu Electronic Technology Co., LTD

Specification

TFT-LCD module

Module(型号)：	FJ040B30M06-A
Customer（客户）：	
Customer P/N（客户型号）：	

Approved by（批准）：	
Qualified（合格）：	Unqualified（不合格）：

PREPARED	CHECKED	APPROVED

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1. Introduction

1.1 Scope of application

This specification applies to the LCD module that is supplied by ShenZhen FangJiu Electronic Technology CO., LTD.
LCD specification: Dots 720xRGBx720
As to basic specification of the driver IC, refer to the IC (NV3051F)
specification and data book.
All material & processing of the LCD module should be Lead Free.

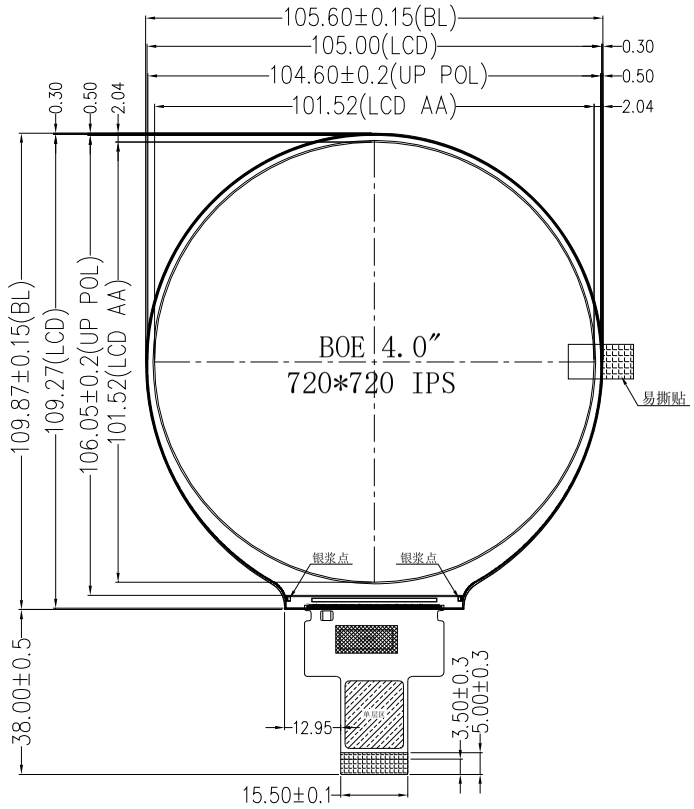
1.2 TFT features:

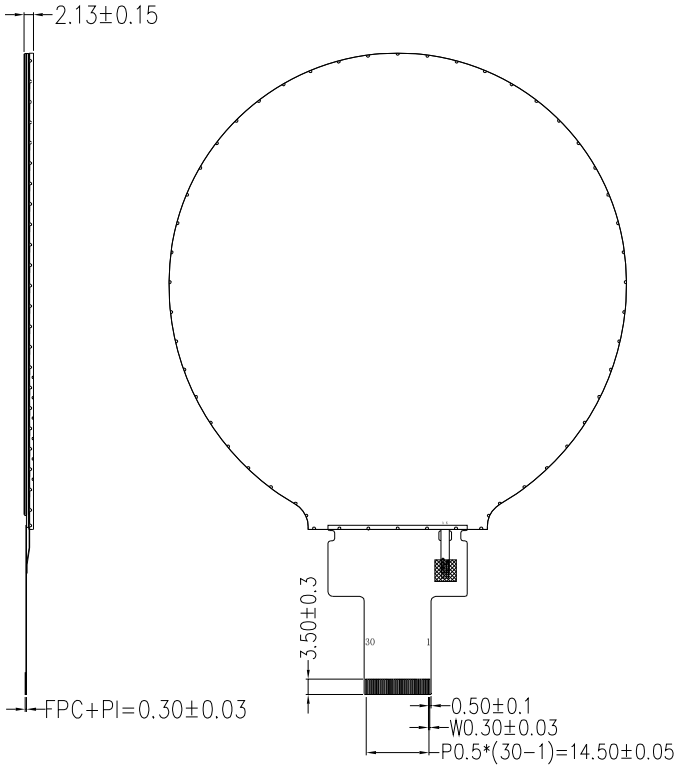
Structure: TFT PANNEL+IC +FPC+BL;
ALL Viewing Type LCD
720 dot-segment and 720 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
4lane MIPI interface

2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	720*3RGB(H)X720(V)	Dots
Pixel arrangement	RGB Vertical Stripe	--
Pixel Pitch (W*H)	0.141H) X 0.141(V)	mm
Active area	101.52(H) x 101.52(V)	mm
Viewing direction	ALL O'CLOCK	-
TFT Driver IC	NV3051F	
TFT interface	4lane MIPI interface	-
Approx. Weight	TBD	g
LCM Size(W*H*T)	105.6(W) ×109.87(H) ×2.13(T)	mm
Touch structure	--	
Touch Driver IC	--	-
Touch Interface	--	

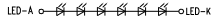
REV	DESCRIPTION	DRG DATE	DRAWN BY
	First Desing	2022.03.15	





TP+LCM:	
NO.	SYMBOL
1	LEDA
2	LEDK
3	LEDK
4	VCI
5	IOVCC
6	RESET
7	TE
8	PWM
9	GND
10	DOP
11	DON
12	GND
13	D1P
14	D1N
15	GND
16	CLKP
17	CLKN
18	GND
19	D2P
20	D2N
21	GND
22	D3P
23	D3N
24	GND
25	TP_INT
26	TP_SDA
27	TP_SCL
28	TP_RESET
29	TP_VCI
30	GND

NOTES:
1. DISPLAY TYPE: 4.0″, 720*720 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: ALL
4. DRIVER IC:NV3051F
5. LCM (White 9 AVG 1/9) :
   Brightness: TBDcd/m^2 (TYP)
   Uniformity:80%(MIN)
6. BACK LIGHT:4 chip white LEDs If=20mA,Vf=16.8V-19.2V
7. OPERATING TEMP: -20° C TO 60° C,STORAGE TEMP: -30° C TO 70° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
   Unspecified Tolerances:±0.20mm
   Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS



IF=20mA Vf=18V

FPC展开出货

深圳市方九电子科技有限公司
Shenzhen Fangjiu Electronic Technology Co., Ltd.

PART NO.:	FJ040B30M06-A			MODULE NO.:	00
DRAWN BY:	LYH	DATE:	2022.03.15	PROJECTION:	
CHECKED BY:		DATE:		SCALE:N.T.S	UNIT: mm
APPROVED BY:		DATE:		SHEET: 1 OF 1	

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+60	°C
LCM Storage Temperature	T_{STG}	-30	+70	°C
Humidity	RH	-	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	1.65	1.8	3.3	V
Supply Voltage for(DC/DC)	VDD	2.7	3.3	3.6	V
Current Consumption	I_{DD}	--	100	--	mA
	$I_{DD\text{-}SLEEP}$	--	150	--	uA

4.2 Back-Light Unit Characeristics

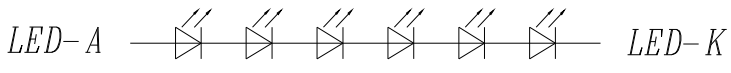
The back-light system is an edge-lighting type with 6 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	16.8	--	19.2	V	-
Forward current	I_F	--	20	-	mA	-
Luminance(With LCD)	Lv	TBD		--	cd/m^2	-
LED life time	N/A	----	30,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

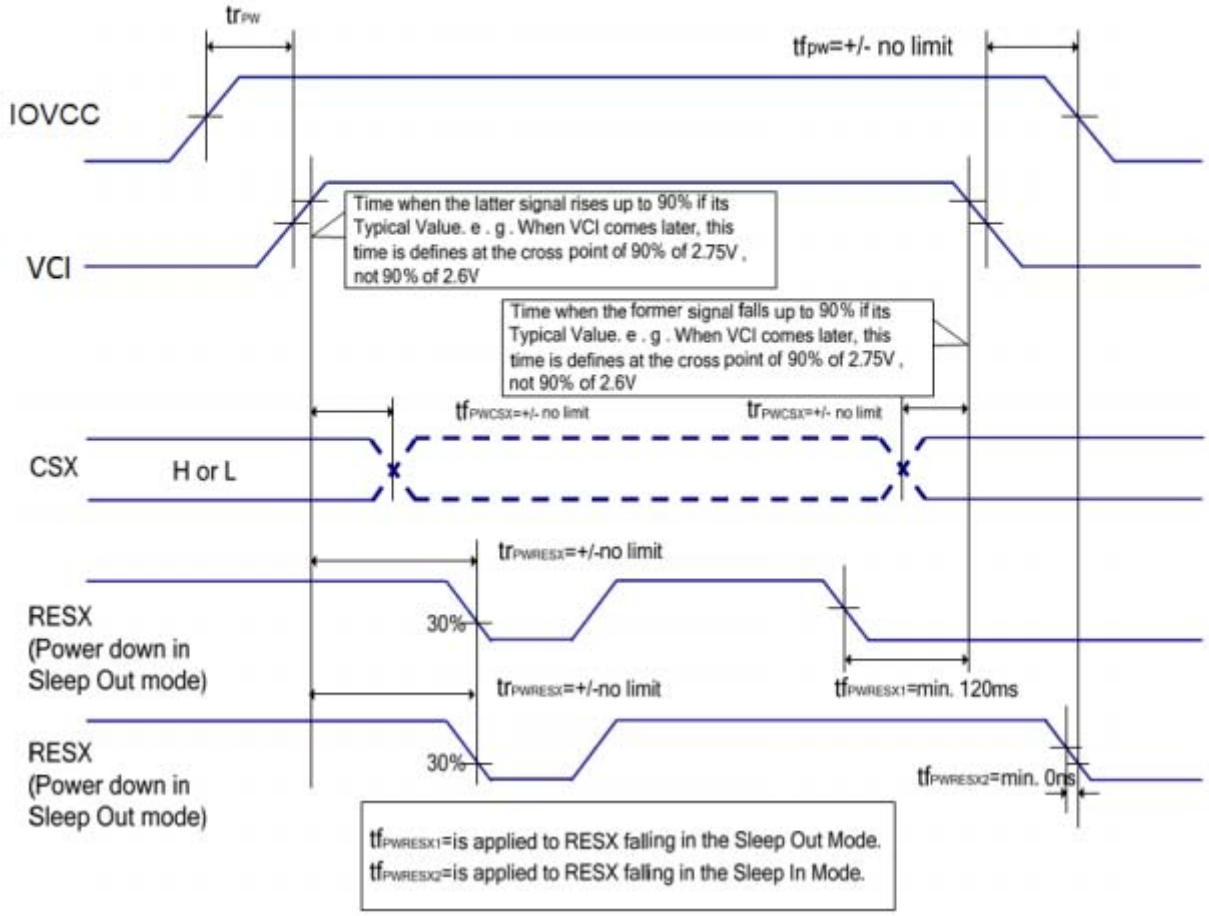
Pin No.	Symbol	LCM Functional	Notes
1	LEDA	Power supply for backlight anode input terminal.	
2	LEDK	Power supply for backlight cathode input terminal.	
3	LEDK	Power supply for backlight cathode input terminal.	
4	VCI	Power Supply For LCD.	
5	IOVCC	power supply for the I/O circuit（1.65~3.3V）	
6	RESET	Reset pin. Setting either pin low initializes the LSI	
7	TE	Tearing effect output pin.	
8	PWM	PWM (Pulse Width Modulation) Signal Of LED Driving.	
9	GND	Power Ground	
10	MIPI_D0P	MIPI-DSI Data differential signal input pins	
11	MIPI_D0N	MIPI-DSI Data differential signal input pins	
12	GND	Power Ground	
13	MIPI_D1P	MIPI-DSI Data differential signal input pins	
14	MIPI_D1N	MIPI-DSI Data differential signal input pins	
15	GND	Power Ground	
16	CLKP	MIPI-DSI CLOCK differential signal input pins	
17	CLKN	MIPI-DSI CLOCK differential signal input pins	
18	GND	Power Ground	
19	MIPI_D2P	MIPI-DSI Data differential signal input pins	
20	MIPI_D2N	MIPI-DSI Data differential signal input pins	
21	GND	Power Ground	
22	MIPI_D3P	MIPI-DSI Data differential signal input pins	
23	MIPI_D3N	MIPI-DSI Data differential signal input pins	
24	GND	Power Ground	
25	CTP_INT	Touch panel interrupt output	
26	CTP_SDA	Touch panel I2C data	
27	CTP_SCL	Touch panel I2C clock	
28	CTP_RESET	Reset pin. Setting either pin low initializes the LSI	
29	CTP_VCI	Power Supply For LCD.	
30	GND	Power Ground	

6. Timing Characteristics

Power On/Off Sequence

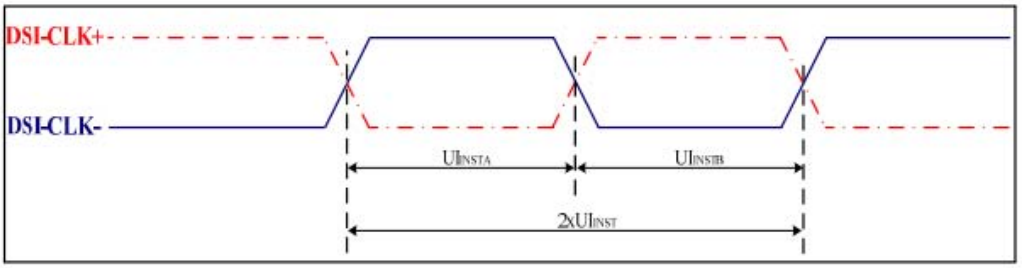
Case 1 – RESX line is held high or unstable by host at power on

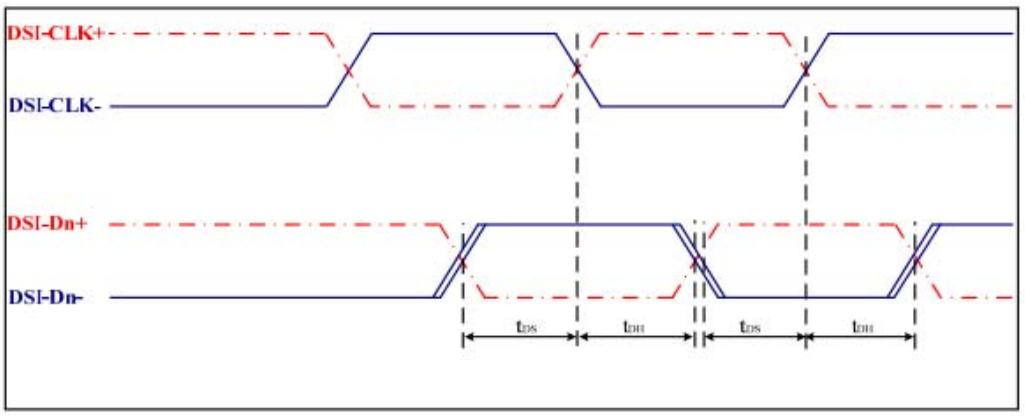
If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



High speed mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Mode						
DSI-CLK+/-	$2Xui_{inst}$	Double UI instantaneous	2.22	-	25	ns
DSI-CLK+/-	UI_{INSTA} , UI_{INSTB}	UI instantaneous Halfs	1.11	-	12.5	ns
DSI-Dn+/-	T_{ds}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	T_{dh}	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	T_{drclk}	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	T_{drdata}	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	T_{dfclk}	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	T_{dfdata}	Differential fall time for data	150	-	0.3UI	ps





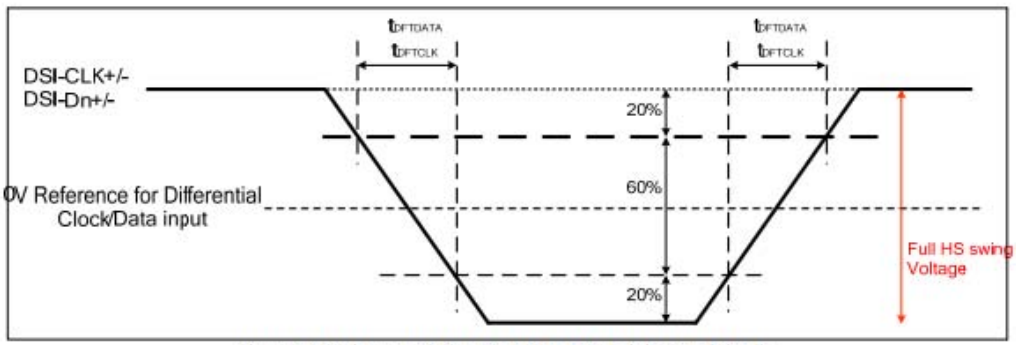


Figure: AC characteristics for MIPI-DSI High speed mode

Low power mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power Mode						
DSI-D0+/-	TLPXM	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU Display Module	50	-	-	ns
DSI- D0+/-	TLPXD	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Modulen MPU	58	-	-	ns
DSI- D0+/-	TTA-SURED	Time-out before the MPU start driving	TLPXD	-	2XTLPXD	ns
DSI- D0+/-	TTA-GETD	Time to drive LP-00 by display module	5XTLPXD	-	-	ns
DSI- D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request – MPU	4XTLPXD	-	-	ns
DSI- D0+/-	Ratio TLPX	Ratio of TLPXM / TLPXD between MCU and display module	2/3	-	3/2	

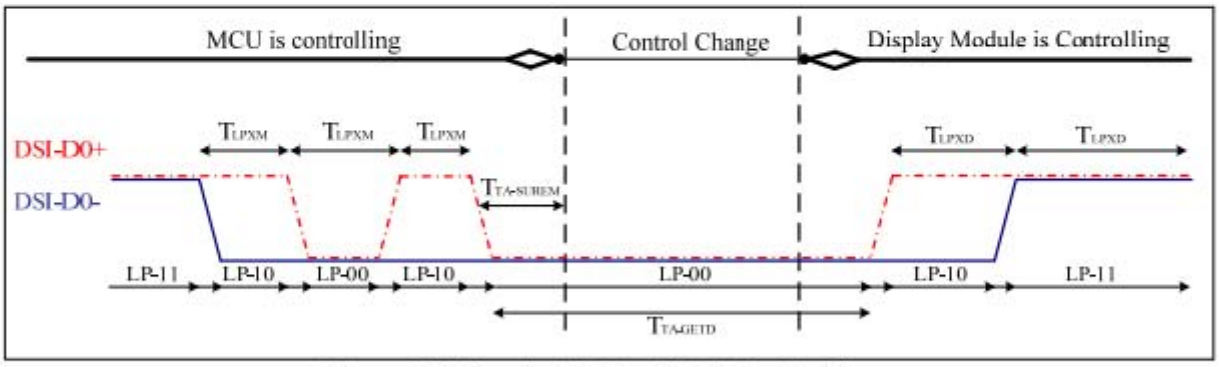


Figure: BTA from the MCU to the Display Module

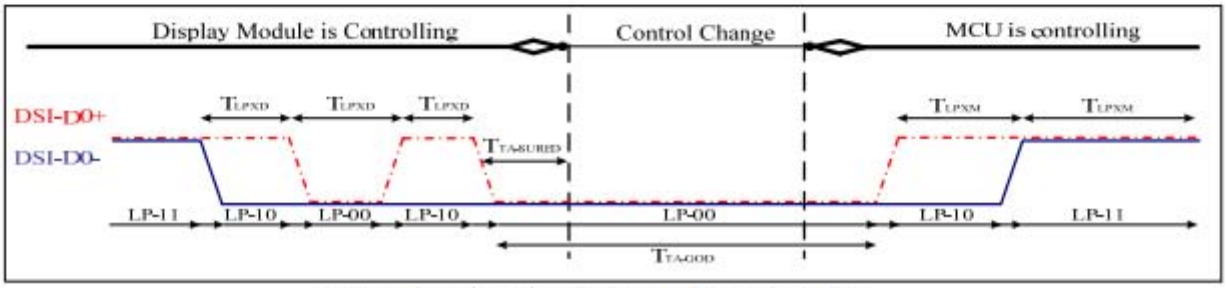


Figure: BTA from the Display Module to the MCU

Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	TLPX	Length of any low-power state period	50	-	-	ns
DSI- Dn+/-	THS- PREPARE	Time to drive LP-00 to prepare for HS transmission	40ns+4UI	-	85ns+6UI	ns
DSI- Dn+/-	THS-PREPARE+THS-ZERO	THS-PREPARE+time to drive HS-0 before the sync sequence	145ns+10UI	-	-	ns
DSI- Dn+/-	TD-TERM- EN	Time to enable Data Lane receiver line termination measured from when Dn crosses VIL(max)	Time for Dn to reach VTERM-EN	-	35ns+4UI	ns
DSI- Dn+/-	THS-SKIP	Time-out at RX to ignore transition period of EoT	40	-	55ns+4UI	ns
DSI- Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI- Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns
DSI- Dn+/-	TeoT	Time from start of THS-TRAIL period to start of LP-11 state	-	-	105ns+12UI	ns

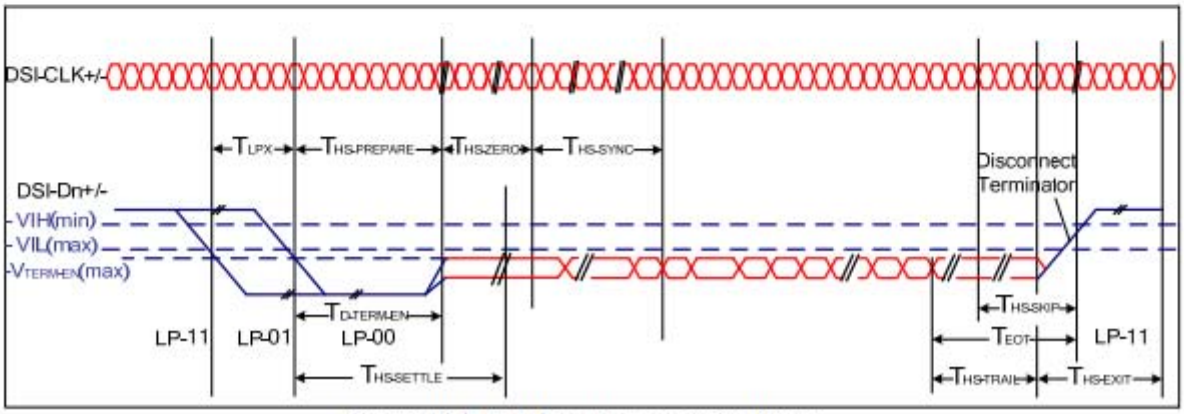


Figure: High Speed Data Transmission Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	TCLK-POST	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60ns+52UI	-	-	ns
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	TCLK-TERM- EN	Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach VTERM-EN	-	38	ns
DSI- CLK+/-	TCLK-PREPARE +TCLK-ZERO	TCLK-PREPARE + time for lead HS-0 drive period before starting Clock	300	-	-	ns
DSI- CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	TeoT	Time from start of TCLK-TRAIL period to start of LP-11 state	-	-	105ns+ 12UI	ns

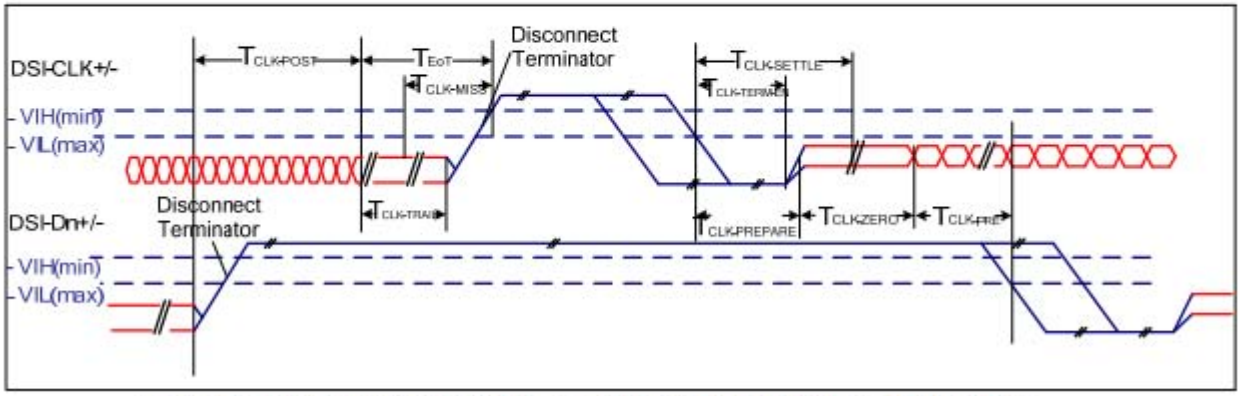
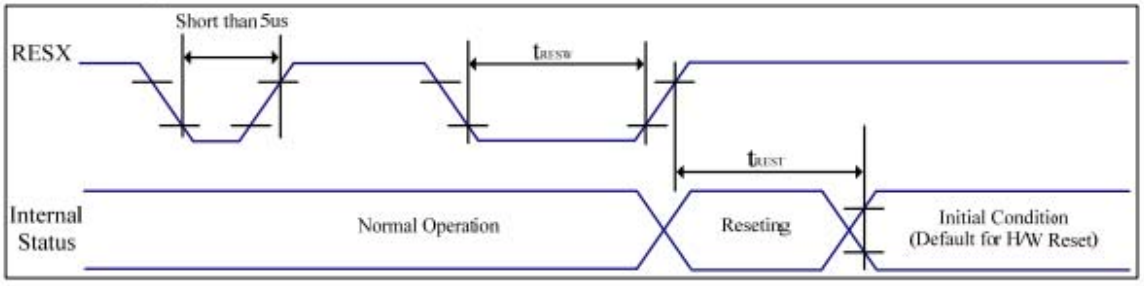


Figure: Switching the clock Lane between clock Transmission and Low Power Mode

Reset timing characteristics



VSS=0V, IOVCC=1.65V to 3.6V, VCI=2.5V to 6.0V, Ta = -30℃ to 70℃

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
T_{resw}	*1) Reset low pulse width	RESX	10	-	-	-	us
T_{rest}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

Table: Reset input timing

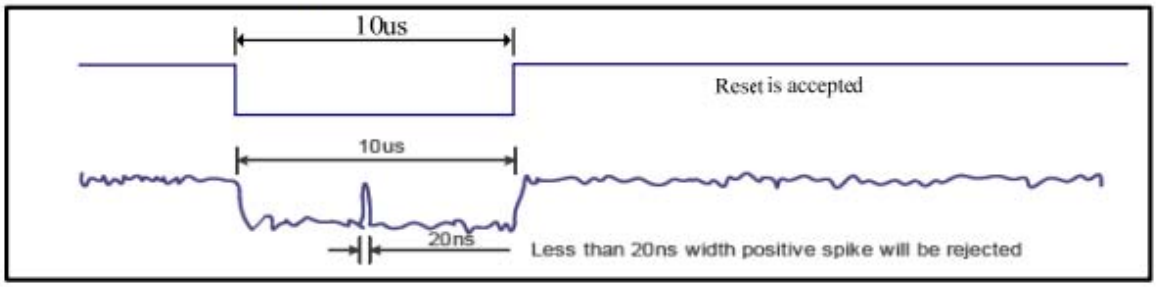
Note 1: Due to an electrostatic discharge on RESX line,spike does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition.)

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode) , then return to default condition for H/W reset.

Note 3: During Reset Complete Time, ID1/ID2/ID3 and VCOM value in OTP will be latched to internal register. After a rising edge of RESX, there is a H/W reset complete time (Trest) which lasted 5ms.The loading operation will be done every time during this reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

7. Optical Characteristics

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	80	85	-	Deg.	Note 1
		Θ_9		80	85	-	Deg.	
	Vertical	Θ_{12}		80	85	-	Deg.	
		Θ_6		80	85	-	Deg.	
Luminance Contrast ratio		CR	Θ = 0° (Center) Normal Viewing Angle	1000	1200	-		Note 2
Transmittance (pol)		T(%)		4.55	5.35	-	%	@Silicate BLU POL:HC+ Clear Note 3
White luminance uniformity		ΔY					%	
White Chromaticity		x_w		0.262	0.292	0.322		CF @C Light Note 4
		y_w		0.307	0.337	0.367		
Reproduction of color	Red	x_R		0.620	0.650	0.680		
		y_R		0.292	0.322	0.352		
	Green	x_G		0.250	0.280	0.310		
		y_G		0.533	0.563	0.593		
	Blue	x_B		0.105	0.135	0.165		
		y_B		0.111	0.141	0.171		
Response Time (Rising + Falling)		T_{RT}	Ta= 25° C Θ = 0°	-	30	35	ms	Note 5

Note :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
2. Contrast measurements shall be made at viewing angle of $\theta = 0°$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIGURE 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the Value with Polarizer(HC+Clear) & silicate BLU (Film structure is on Table 4.1)
4. The color chromaticity coordinates specified in the above Table shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
5. The electro-optical response time measurements shall be made as **FIGURE 1** shown in Appendix. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Tf.

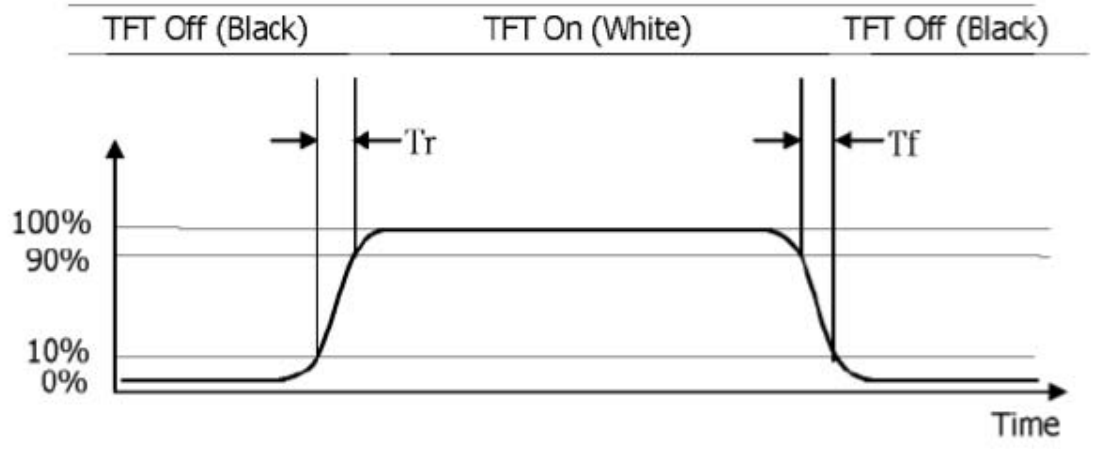


Figure1 Response Time Testing

8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+70°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+60°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH /96H	
6	Thermal and cold shock	Static state，-20℃（30min）~70℃（30min），50 cycles	

9. Packing Method----TBD

- END -