ST7797

400RGB x 400 16.7M Color without Display Ram Single-Chip TFT Controller/Driver

Datasheet

Version 1.1

2018/07

Sitronix Technology Corporation

LIST OF CONTENT

1 GENERAL DESCRIPTION

The ST7797 is a single-chip controller/driver for 16.7M-color, graphic type TFT-LCD. The 400-channel source driver has true 8-bit resolution, which generates 64 Gamma-corrected values by an internal D/A converter. The ST7797 is capable of connecting directly to an external microprocessor, and provides MIPI interface. In addition, because of the integrated power supply circuit necessary to drive liquid crystal; it is possible to make a display system with fewest components.

2 FEATURES

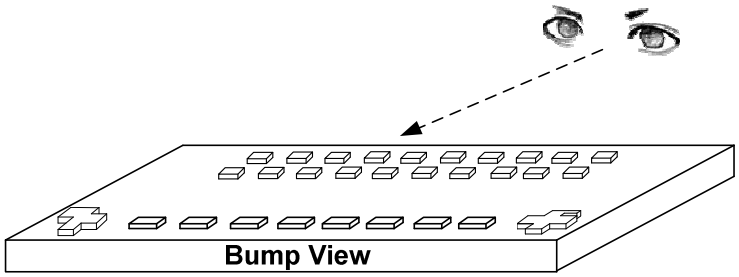
- Single chip TFT-LCD Controller/Driver without Display RAM
- Display Resolution:
  - 400*RGB (H) *400(V)
  - 360*RGB (H) *360(V)
  - 320*RGB (H) *320(V)
  - 280*RGB (H) *280(V)
  - 240*RGB (H) *240(V)
  - 128*RGB (H) *128(V)
- LCD Driver Output Circuits
  - Source Outputs: 400 RGB Channels
  - Support gate control signals to gate driver in the panel
- Display Colors (Color Mode)
  - Idle Mode:8-colors
  - 2-color idle mode(1-bpp RAM) (Picture maximum compression size < 4k bytes)
- Programmable Pixel Color Format (Color Depth) for Various Display Data Input Format
  - 16-bit/pixel: RGB=(565) 65K color
  - 18-bit/pixel: RGB=(666) 262K color
  - 24-bit/pixel: RGB=(888) 16.7M color
- Interface
  - MIPI Video Mode
- Display Features
  - 1Gamma (64 graylevels)
  - SRE Function(enhancement CR)
- On Chip Build-In Circuits
  - DC/DC Converter
  - Non-Volatile (NV) Memory to Store Initial Register Setting and Factory Default Value (Module ID, Module Version, etc)
  - Adjustable VCOM Generation
  - Timing Controller
- Build-In NV Memory for LCD Initial Register Setting
  - OTP to store VCOM and ID1~ID3
- Driving Algorithm
  - 1-dot/2-dot Inversion
  - Column Inversion

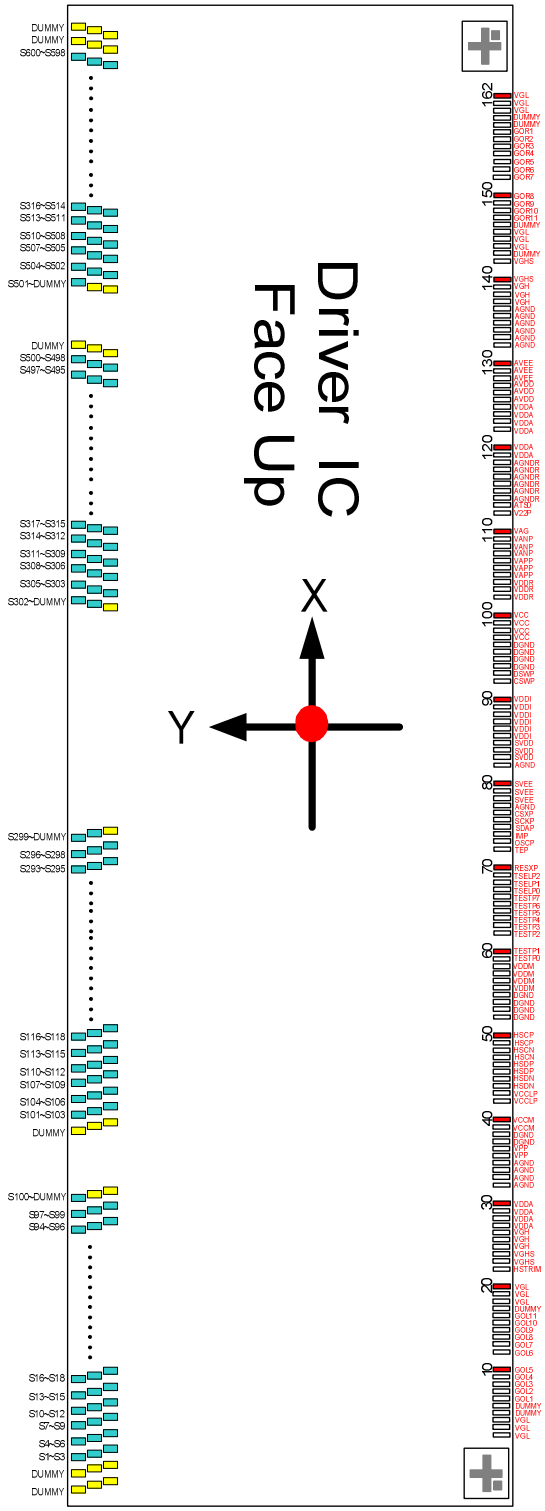
- Wide Supply Voltage Range
  - I/O Voltage (VDDI to DGND): 1.65V ~ 3.3V (VDDI≦VDD)
    In VCCBYPASS Mode: VDDI=1.8v
  - Voltage for Digital Circuit (VDD to DGND): 2.6V ~ 3.3V
  - Voltage for Analog Circuit (VDDA to AGND): 2.6V ~ 3.3V
- On-Chip Power System
  - VCOM Level: AGND
- COG Type
  - 3 Stagger 11um
- Operate temperature range: −30ºC to +85 ºC
- Power saving modes
  - Deep standby mode
  - Sleep mode
  - Low frame mode 15Hz
- Output Power
  - Gamma(+) voltage range: 3.7V~6.4V
  - Gamma(-) voltage range:-4V~-1.2V
  - VGHO voltage range:12.6V~15.5V
  - VGLO voltage range: -8.3V~-11.8V
- Others
  - Zero-Cap
  - GIP + Dual-gate driving
  - OTP

3 PAD ARRANGEMENT

3.1 Output Bump Dimension

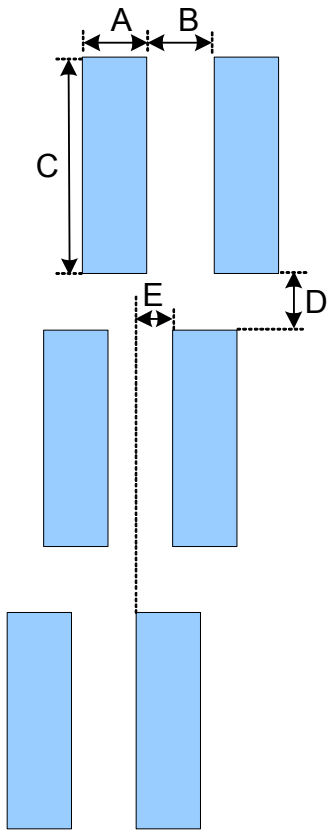
Au bump height	9um
Au bump size	15μmx75μm Gate : GOL1~GOL10 GOR1~GOR10 Source : S1~S600
	30μmx75μm (Pad1 to Pad162)





3.2 Bump Dimension

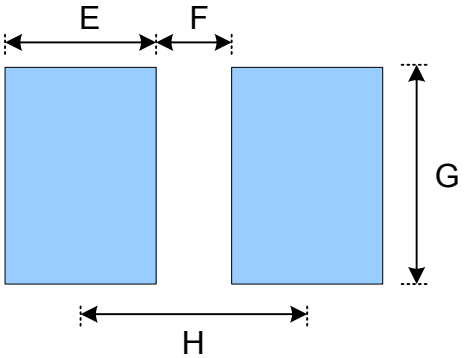
●Output Pads



Symbol	Item	Size
A	Bump Width	15 um
B	Bump Gap 1 (Horizontal)	18 um
C	Bump Height	75 um
D	Bump Gap 2 (Vertical)	25 um
E	Bump Pitch	11um

●Input Pads

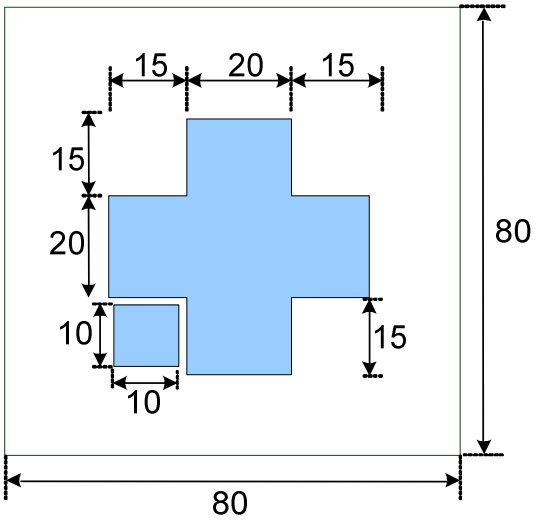
Pad No.1~162



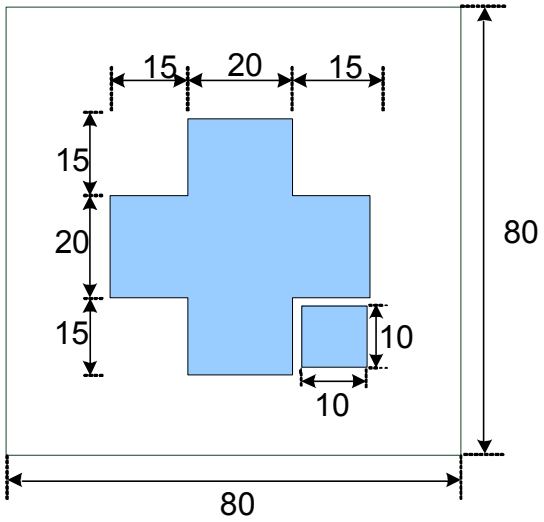
Symbol	Item	Size
E	Bump Width	30 um
F	Bump Gap	15 um
G	Bump Height	75 um
H	Bump Pitch	45 um

3.3 Alignment Mark Dimension

● **Alignment Mark Left: L(X,Y)=(-3707, -352)**



● **Alignment Mark Right: R(X,Y)= (3707, -352)**



3.4 Chip Information

Chip size	7600um x 900um
Chip thickness	250um
Pad Location	Pad center
Coordinate Origin	Chip center

4 PAD CENTER COORDINATES

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	VGL	-3622.5	-349.5	34	AGND	-2137.5	-349.5
2	VGL	-3577.5	-349.5	35	VPP	-2092.5	-349.5
3	VGL	-3532.5	-349.5	36	VPP	-2047.5	-349.5
4	DUMMY	-3487.5	-349.5	37	DGND	-2002.5	-349.5
5	DUMMY	-3442.5	-349.5	38	DGND	-1957.5	-349.5
6	GOL1	-3397.5	-349.5	39	VCCM	-1912.5	-349.5
7	GOL2	-3352.5	-349.5	40	VCCM	-1867.5	-349.5
8	GOL3	-3307.5	-349.5	41	VCCLP	-1822.5	-349.5
9	GOL4	-3262.5	-349.5	42	VCCLP	-1777.5	-349.5
10	GOL5	-3217.5	-349.5	43	HSDN	-1732.5	-349.5
11	GOL6	-3172.5	-349.5	44	HSDN	-1687.5	-349.5
12	GOL7	-3127.5	-349.5	45	HSDP	-1642.5	-349.5
13	GOL8	-3082.5	-349.5	46	HSDP	-1597.5	-349.5
14	GOL9	-3037.5	-349.5	47	HSCN	-1552.5	-349.5
15	GOL10	-2992.5	-349.5	48	HSCN	-1507.5	-349.5
16	GLTEST	-2947.5	-349.5	49	HSCP	-1462.5	-349.5
17	DUMMY	-2902.5	-349.5	50	HSCP	-1417.5	-349.5
18	VGL	-2857.5	-349.5	51	DGND	-1372.5	-349.5
19	VGL	-2812.5	-349.5	52	DGND	-1327.5	-349.5
20	VGL	-2767.5	-349.5	53	DGND	-1282.5	-349.5
21	HSTRIM	-2722.5	-349.5	54	DGND	-1237.5	-349.5
22	VGHS	-2677.5	-349.5	55	VDDM	-1192.5	-349.5
23	VGHS	-2632.5	-349.5	56	VDDM	-1147.5	-349.5
24	VGH	-2587.5	-349.5	57	VDDM	-1102.5	-349.5
25	VGH	-2542.5	-349.5	58	VDDM	-1057.5	-349.5
26	VGH	-2497.5	-349.5	59	TESTP0	-1012.5	-349.5
27	VDDA	-2452.5	-349.5	60	TESTP1	-967.5	-349.5
28	VDDA	-2407.5	-349.5	61	TESTP2	-922.5	-349.5
29	VDDA	-2362.5	-349.5	62	TESTP3	-877.5	-349.5
30	VDDA	-2317.5	-349.5	63	TESTP4	-832.5	-349.5
31	AGND	-2272.5	-349.5	64	TESTP5	-787.5	-349.5
32	AGND	-2227.5	-349.5	65	TESTP6	-742.5	-349.5
33	AGND	-2182.5	-349.5	66	TESTP7	-697.5	-349.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
67	TSELP0	-652.5	-349.5	101	VDDR	877.5	-349.5
68	TSELP1	-607.5	-349.5	102	VDDR	922.5	-349.5
69	TSELP2	-562.5	-349.5	103	VDDR	967.5	-349.5
70	RESXP	-517.5	-349.5	104	VAPP	1012.5	-349.5
71	TEP	-472.5	-349.5	105	VAPP	1057.5	-349.5
72	OSCP	-427.5	-349.5	106	VAPP	1102.5	-349.5
73	IMP	-382.5	-349.5	107	VANP	1147.5	-349.5
74	SDAP	-337.5	-349.5	108	VANP	1192.5	-349.5
75	SCKP	-292.5	-349.5	109	VANP	1237.5	-349.5
76	CSXP	-247.5	-349.5	110	VAG	1282.5	-349.5
77	AGND	-202.5	-349.5	111	V22P	1327.5	-349.5
78	SVEE	-157.5	-349.5	112	ATS0	1372.5	-349.5
79	SVEE	-112.5	-349.5	113	AGNDR	1417.5	-349.5
80	SVEE	-67.5	-349.5	114	AGNDR	1462.5	-349.5
81	AGND	-22.5	-349.5	115	AGNDR	1507.5	-349.5
82	SVDD	22.5	-349.5	116	AGNDR	1552.5	-349.5
83	SVDD	67.5	-349.5	117	AGNDR	1597.5	-349.5
84	SVDD	112.5	-349.5	118	AGNDR	1642.5	-349.5
85	VDDI	157.5	-349.5	119	VDDA	1687.5	-349.5
86	VDDI	202.5	-349.5	120	VDDA	1732.5	-349.5
87	VDDI	247.5	-349.5	121	VDDA	1777.5	-349.5
88	VDDI	292.5	-349.5	122	VDDA	1822.5	-349.5
89	VDDI	337.5	-349.5	123	VDDA	1867.5	-349.5
90	VDDI	382.5	-349.5	124	VDDA	1912.5	-349.5
91	CSWP	427.5	-349.5	125	AVDD	1957.5	-349.5
92	DSWP	472.5	-349.5	126	AVDD	2002.5	-349.5
93	DGND	517.5	-349.5	127	AVDD	2047.5	-349.5
94	DGND	562.5	-349.5	128	AVEE	2092.5	-349.5
95	DGND	607.5	-349.5	129	AVEE	2137.5	-349.5
96	DGND	652.5	-349.5	130	AVEE	2182.5	-349.5
97	VCC	697.5	-349.5	131	AGND	2227.5	-349.5
98	VCC	742.5	-349.5	132	AGND	2272.5	-349.5
99	VCC	787.5	-349.5	133	AGND	2317.5	-349.5
100	VCC	832.5	-349.5	134	AGND	2362.5	-349.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
135	AGND	2407.5	-349.5	169	S600	3664	349.5
136	AGND	2452.5	-349.5	170	S599	3653	249.5
137	VGH	2497.5	-349.5	171	S598	3642	149.5
138	VGH	2542.5	-349.5	172	S597	3631	349.5
139	VGH	2587.5	-349.5	173	S596	3620	249.5
140	VGHS	2632.5	-349.5	174	S595	3609	149.5
141	VGHS	2677.5	-349.5	175	S594	3598	349.5
142	DUMMY	2722.5	-349.5	176	S593	3587	249.5
143	VGL	2767.5	-349.5	177	S592	3576	149.5
144	VGL	2812.5	-349.5	178	S591	3565	349.5
145	VGL	2857.5	-349.5	179	S590	3554	249.5
146	DUMMY	2902.5	-349.5	180	S589	3543	149.5
147	GRTEST	2947.5	-349.5	181	S588	3532	349.5
148	GOR10	2992.5	-349.5	182	S587	3521	249.5
149	GOR9	3037.5	-349.5	183	S586	3510	149.5
150	GOR8	3082.5	-349.5	184	S585	3499	349.5
151	GOR7	3127.5	-349.5	185	S584	3488	249.5
152	GOR6	3172.5	-349.5	186	S583	3477	149.5
153	GOR5	3217.5	-349.5	187	S582	3466	349.5
154	GOR4	3262.5	-349.5	188	S581	3455	249.5
155	GOR3	3307.5	-349.5	189	S580	3444	149.5
156	GOR2	3352.5	-349.5	190	S579	3433	349.5
157	GOR1	3397.5	-349.5	191	S578	3422	249.5
158	DUMMY	3442.5	-349.5	192	S577	3411	149.5
159	DUMMY	3487.5	-349.5	193	S576	3400	349.5
160	VGL	3532.5	-349.5	194	S575	3389	249.5
161	VGL	3577.5	-349.5	195	S574	3378	149.5
162	VGL	3622.5	-349.5	196	S573	3367	349.5
163	DUMMY	3730	349.5	197	S572	3356	249.5
164	DUMMY	3719	249.5	198	S571	3345	149.5
165	DUMMY	3708	149.5	199	S570	3334	349.5
166	DUMMY	3697	349.5	200	S569	3323	249.5
167	DUMMY	3686	249.5	201	S568	3312	149.5
168	DUMMY	3675	149.5	202	S567	3301	349.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
203	S566	3290	249.5	237	S532	2916	149.5
204	S565	3279	149.5	238	S531	2905	349.5
205	S564	3268	349.5	239	S530	2894	249.5
206	S563	3257	249.5	240	S529	2883	149.5
207	S562	3246	149.5	241	S528	2872	349.5
208	S561	3235	349.5	242	S527	2861	249.5
209	S560	3224	249.5	243	S526	2850	149.5
210	S559	3213	149.5	244	S525	2839	349.5
211	S558	3202	349.5	245	S524	2828	249.5
212	S557	3191	249.5	246	S523	2817	149.5
213	S556	3180	149.5	247	S522	2806	349.5
214	S555	3169	349.5	248	S521	2795	249.5
215	S554	3158	249.5	249	S520	2784	149.5
216	S553	3147	149.5	250	S519	2773	349.5
217	S552	3136	349.5	251	S518	2762	249.5
218	S551	3125	249.5	252	S517	2751	149.5
219	S550	3114	149.5	253	S516	2740	349.5
220	S549	3103	349.5	254	S515	2729	249.5
221	S548	3092	249.5	255	S514	2718	149.5
222	S547	3081	149.5	256	S513	2707	349.5
223	S546	3070	349.5	257	S512	2696	249.5
224	S545	3059	249.5	258	S511	2685	149.5
225	S544	3048	149.5	259	S510	2674	349.5
226	S543	3037	349.5	260	S509	2663	249.5
227	S542	3026	249.5	261	S508	2652	149.5
228	S541	3015	149.5	262	S507	2641	349.5
229	S540	3004	349.5	263	S506	2630	249.5
230	S539	2993	249.5	264	S505	2619	149.5
231	S538	2982	149.5	265	S504	2608	349.5
232	S537	2971	349.5	266	S503	2597	249.5
233	S536	2960	249.5	267	S502	2586	149.5
234	S535	2949	149.5	268	S501	2575	349.5
235	S534	2938	349.5	269	DUMMY	2564	249.5
236	S533	2927	249.5	270	DUMMY	2553	149.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
271	DUMMY	2373	349.5	305	S469	1999	249.5
272	DUMMY	2362	249.5	306	S468	1988	149.5
273	DUMMY	2351	149.5	307	S467	1977	349.5
274	S500	2340	349.5	308	S466	1966	249.5
275	S499	2329	249.5	309	S465	1955	149.5
276	S498	2318	149.5	310	S464	1944	349.5
277	S497	2307	349.5	311	S463	1933	249.5
278	S496	2296	249.5	312	S462	1922	149.5
279	S495	2285	149.5	313	S461	1911	349.5
280	S494	2274	349.5	314	S460	1900	249.5
281	S493	2263	249.5	315	S459	1889	149.5
282	S492	2252	149.5	316	S458	1878	349.5
283	S491	2241	349.5	317	S457	1867	249.5
284	S490	2230	249.5	318	S456	1856	149.5
285	S489	2219	149.5	319	S455	1845	349.5
286	S488	2208	349.5	320	S454	1834	249.5
287	S487	2197	249.5	321	S453	1823	149.5
288	S486	2186	149.5	322	S452	1812	349.5
289	S485	2175	349.5	323	S451	1801	249.5
290	S484	2164	249.5	324	S450	1790	149.5
291	S483	2153	149.5	325	S449	1779	349.5
292	S482	2142	349.5	326	S448	1768	249.5
293	S481	2131	249.5	327	S447	1757	149.5
294	S480	2120	149.5	328	S446	1746	349.5
295	S479	2109	349.5	329	S445	1735	249.5
296	S478	2098	249.5	330	S444	1724	149.5
297	S477	2087	149.5	331	S443	1713	349.5
298	S476	2076	349.5	332	S442	1702	249.5
299	S475	2065	249.5	333	S441	1691	149.5
300	S474	2054	149.5	334	S440	1680	349.5
301	S473	2043	349.5	335	S439	1669	249.5
302	S472	2032	249.5	336	S438	1658	149.5
303	S471	2021	149.5	337	S437	1647	349.5
304	S470	2010	349.5	338	S436	1636	249.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
339	S435	1625	149.5	373	S401	1251	349.5
340	S434	1614	349.5	374	S400	1240	249.5
341	S433	1603	249.5	375	S399	1229	149.5
342	S432	1592	149.5	376	S398	1218	349.5
343	S431	1581	349.5	377	S397	1207	249.5
344	S430	1570	249.5	378	S396	1196	149.5
345	S429	1559	149.5	379	S395	1185	349.5
346	S428	1548	349.5	380	S394	1174	249.5
347	S427	1537	249.5	381	S393	1163	149.5
348	S426	1526	149.5	382	S392	1152	349.5
349	S425	1515	349.5	383	S391	1141	249.5
350	S424	1504	249.5	384	S390	1130	149.5
351	S423	1493	149.5	385	S389	1119	349.5
352	S422	1482	349.5	386	S388	1108	249.5
353	S421	1471	249.5	387	S387	1097	149.5
354	S420	1460	149.5	388	S386	1086	349.5
355	S419	1449	349.5	389	S385	1075	249.5
356	S418	1438	249.5	390	S384	1064	149.5
357	S417	1427	149.5	391	S383	1053	349.5
358	S416	1416	349.5	392	S382	1042	249.5
359	S415	1405	249.5	393	S381	1031	149.5
360	S414	1394	149.5	394	S380	1020	349.5
361	S413	1383	349.5	395	S379	1009	249.5
362	S412	1372	249.5	396	S378	998	149.5
363	S411	1361	149.5	397	S377	987	349.5
364	S410	1350	349.5	398	S376	976	249.5
365	S409	1339	249.5	399	S375	965	149.5
366	S408	1328	149.5	400	S374	954	349.5
367	S407	1317	349.5	401	S373	943	249.5
368	S406	1306	249.5	402	S372	932	149.5
369	S405	1295	149.5	403	S371	921	349.5
370	S404	1284	349.5	404	S370	910	249.5
371	S403	1273	249.5	405	S369	899	149.5
372	S402	1262	149.5	406	S368	888	349.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
407	S367	877	249.5	441	S333	503	149.5
408	S366	866	149.5	442	S332	492	349.5
409	S365	855	349.5	443	S331	481	249.5
410	S364	844	249.5	444	S330	470	149.5
411	S363	833	149.5	445	S329	459	349.5
412	S362	822	349.5	446	S328	448	249.5
413	S361	811	249.5	447	S327	437	149.5
414	S360	800	149.5	448	S326	426	349.5
415	S359	789	349.5	449	S325	415	249.5
416	S358	778	249.5	450	S324	404	149.5
417	S357	767	149.5	451	S323	393	349.5
418	S356	756	349.5	452	S322	382	249.5
419	S355	745	249.5	453	S321	371	149.5
420	S354	734	149.5	454	S320	360	349.5
421	S353	723	349.5	455	S319	349	249.5
422	S352	712	249.5	456	S318	338	149.5
423	S351	701	149.5	457	S317	327	349.5
424	S350	690	349.5	458	S316	316	249.5
425	S349	679	249.5	459	S315	305	149.5
426	S348	668	149.5	460	S314	294	349.5
427	S347	657	349.5	461	S313	283	249.5
428	S346	646	249.5	462	S312	272	149.5
429	S345	635	149.5	463	S311	261	349.5
430	S344	624	349.5	464	S310	250	249.5
431	S343	613	249.5	465	S309	239	149.5
432	S342	602	149.5	466	S308	228	349.5
433	S341	591	349.5	467	S307	217	249.5
434	S340	580	249.5	468	S306	206	149.5
435	S339	569	149.5	469	S305	195	349.5
436	S338	558	349.5	470	S304	184	249.5
437	S337	547	249.5	471	S303	173	149.5
438	S336	536	149.5	472	S302	162	349.5
439	S335	525	349.5	473	S301	151	249.5
440	S334	514	249.5	474	DUMMY	140	149.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
475	DUMMY	-140	149.5	509	S267	-514	249.5
476	S300	-151	249.5	510	S266	-525	349.5
477	S299	-162	349.5	511	S265	-536	149.5
478	S298	-173	149.5	512	S264	-547	249.5
479	S297	-184	249.5	513	S263	-558	349.5
480	S296	-195	349.5	514	S262	-569	149.5
481	S295	-206	149.5	515	S261	-580	249.5
482	S294	-217	249.5	516	S260	-591	349.5
483	S293	-228	349.5	517	S259	-602	149.5
484	S292	-239	149.5	518	S258	-613	249.5
485	S291	-250	249.5	519	S257	-624	349.5
486	S290	-261	349.5	520	S256	-635	149.5
487	S289	-272	149.5	521	S255	-646	249.5
488	S288	-283	249.5	522	S254	-657	349.5
489	S287	-294	349.5	523	S253	-668	149.5
490	S286	-305	149.5	524	S252	-679	249.5
491	S285	-316	249.5	525	S251	-690	349.5
492	S284	-327	349.5	526	S250	-701	149.5
493	S283	-338	149.5	527	S249	-712	249.5
494	S282	-349	249.5	528	S248	-723	349.5
495	S281	-360	349.5	529	S247	-734	149.5
496	S280	-371	149.5	530	S246	-745	249.5
497	S279	-382	249.5	531	S245	-756	349.5
498	S278	-393	349.5	532	S244	-767	149.5
499	S277	-404	149.5	533	S243	-778	249.5
500	S276	-415	249.5	534	S242	-789	349.5
501	S275	-426	349.5	535	S241	-800	149.5
502	S274	-437	149.5	536	S240	-811	249.5
503	S273	-448	249.5	537	S239	-822	349.5
504	S272	-459	349.5	538	S238	-833	149.5
505	S271	-470	149.5	539	S237	-844	249.5
506	S270	-481	249.5	540	S236	-855	349.5
507	S269	-492	349.5	541	S235	-866	149.5
508	S268	-503	149.5	542	S234	-877	249.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
543	S233	-888	349.5	577	S199	-1262	149.5
544	S232	-899	149.5	578	S198	-1273	249.5
545	S231	-910	249.5	579	S197	-1284	349.5
546	S230	-921	349.5	580	S196	-1295	149.5
547	S229	-932	149.5	581	S195	-1306	249.5
548	S228	-943	249.5	582	S194	-1317	349.5
549	S227	-954	349.5	583	S193	-1328	149.5
550	S226	-965	149.5	584	S192	-1339	249.5
551	S225	-976	249.5	585	S191	-1350	349.5
552	S224	-987	349.5	586	S190	-1361	149.5
553	S223	-998	149.5	587	S189	-1372	249.5
554	S222	-1009	249.5	588	S188	-1383	349.5
555	S221	-1020	349.5	589	S187	-1394	149.5
556	S220	-1031	149.5	590	S186	-1405	249.5
557	S219	-1042	249.5	591	S185	-1416	349.5
558	S218	-1053	349.5	592	S184	-1427	149.5
559	S217	-1064	149.5	593	S183	-1438	249.5
560	S216	-1075	249.5	594	S182	-1449	349.5
561	S215	-1086	349.5	595	S181	-1460	149.5
562	S214	-1097	149.5	596	S180	-1471	249.5
563	S213	-1108	249.5	597	S179	-1482	349.5
564	S212	-1119	349.5	598	S178	-1493	149.5
565	S211	-1130	149.5	599	S177	-1504	249.5
566	S210	-1141	249.5	600	S176	-1515	349.5
567	S209	-1152	349.5	601	S175	-1526	149.5
568	S208	-1163	149.5	602	S174	-1537	249.5
569	S207	-1174	249.5	603	S173	-1548	349.5
570	S206	-1185	349.5	604	S172	-1559	149.5
571	S205	-1196	149.5	605	S171	-1570	249.5
572	S204	-1207	249.5	606	S170	-1581	349.5
573	S203	-1218	349.5	607	S169	-1592	149.5
574	S202	-1229	149.5	608	S168	-1603	249.5
575	S201	-1240	249.5	609	S167	-1614	349.5
576	S200	-1251	349.5	610	S166	-1625	149.5

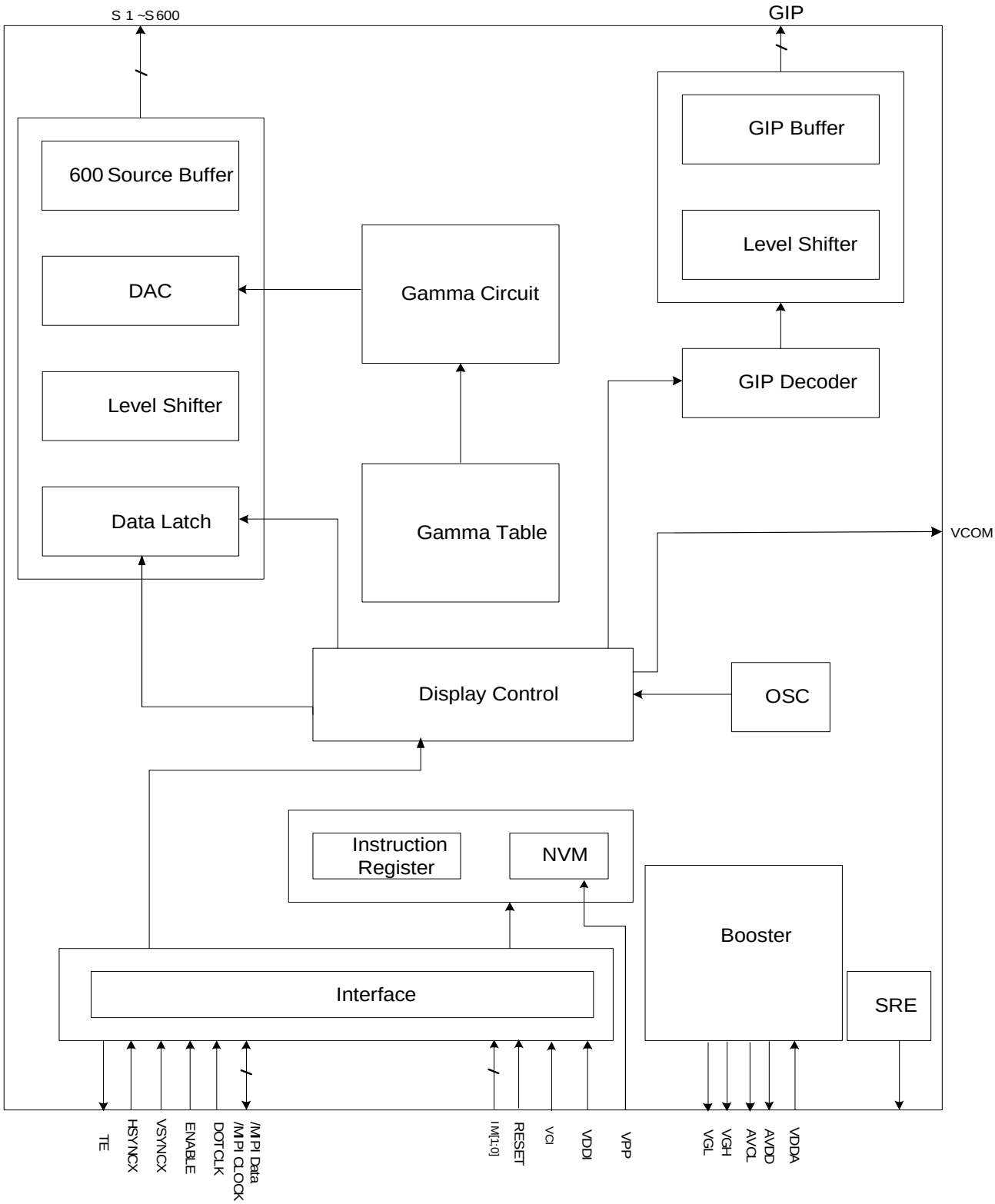
PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
611	S165	-1636	249.5	645	S131	-2010	349.5
612	S164	-1647	349.5	646	S130	-2021	149.5
613	S163	-1658	149.5	647	S129	-2032	249.5
614	S162	-1669	249.5	648	S128	-2043	349.5
615	S161	-1680	349.5	649	S127	-2054	149.5
616	S160	-1691	149.5	650	S126	-2065	249.5
617	S159	-1702	249.5	651	S125	-2076	349.5
618	S158	-1713	349.5	652	S124	-2087	149.5
619	S157	-1724	149.5	653	S123	-2098	249.5
620	S156	-1735	249.5	654	S122	-2109	349.5
621	S155	-1746	349.5	655	S121	-2120	149.5
622	S154	-1757	149.5	656	S120	-2131	249.5
623	S153	-1768	249.5	657	S119	-2142	349.5
624	S152	-1779	349.5	658	S118	-2153	149.5
625	S151	-1790	149.5	659	S117	-2164	249.5
626	S150	-1801	249.5	660	S116	-2175	349.5
627	S149	-1812	349.5	661	S115	-2186	149.5
628	S148	-1823	149.5	662	S114	-2197	249.5
629	S147	-1834	249.5	663	S113	-2208	349.5
630	S146	-1845	349.5	664	S112	-2219	149.5
631	S145	-1856	149.5	665	S111	-2230	249.5
632	S144	-1867	249.5	666	S110	-2241	349.5
633	S143	-1878	349.5	667	S109	-2252	149.5
634	S142	-1889	149.5	668	S108	-2263	249.5
635	S141	-1900	249.5	669	S107	-2274	349.5
636	S140	-1911	349.5	670	S106	-2285	149.5
637	S139	-1922	149.5	671	S105	-2296	249.5
638	S138	-1933	249.5	672	S104	-2307	349.5
639	S137	-1944	349.5	673	S103	-2318	149.5
640	S136	-1955	149.5	674	S102	-2329	249.5
641	S135	-1966	249.5	675	S101	-2340	349.5
642	S134	-1977	349.5	676	DUMMY	-2351	149.5
643	S133	-1988	149.5	677	DUMMY	-2362	249.5
644	S132	-1999	249.5	678	DUMMY	-2373	349.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
679	DUMMY	-2553	149.5	713	S68	-2927	249.5
680	DUMMY	-2564	249.5	714	S67	-2938	349.5
681	S100	-2575	349.5	715	S66	-2949	149.5
682	S99	-2586	149.5	716	S65	-2960	249.5
683	S98	-2597	249.5	717	S64	-2971	349.5
684	S97	-2608	349.5	718	S63	-2982	149.5
685	S96	-2619	149.5	719	S62	-2993	249.5
686	S95	-2630	249.5	720	S61	-3004	349.5
687	S94	-2641	349.5	721	S60	-3015	149.5
688	S93	-2652	149.5	722	S59	-3026	249.5
689	S92	-2663	249.5	723	S58	-3037	349.5
690	S91	-2674	349.5	724	S57	-3048	149.5
691	S90	-2685	149.5	725	S56	-3059	249.5
692	S89	-2696	249.5	726	S55	-3070	349.5
693	S88	-2707	349.5	727	S54	-3081	149.5
694	S87	-2718	149.5	728	S53	-3092	249.5
695	S86	-2729	249.5	729	S52	-3103	349.5
696	S85	-2740	349.5	730	S51	-3114	149.5
697	S84	-2751	149.5	731	S50	-3125	249.5
698	S83	-2762	249.5	732	S49	-3136	349.5
699	S82	-2773	349.5	733	S48	-3147	149.5
700	S81	-2784	149.5	734	S47	-3158	249.5
701	S80	-2795	249.5	735	S46	-3169	349.5
702	S79	-2806	349.5	736	S45	-3180	149.5
703	S78	-2817	149.5	737	S44	-3191	249.5
704	S77	-2828	249.5	738	S43	-3202	349.5
705	S76	-2839	349.5	739	S42	-3213	149.5
706	S75	-2850	149.5	740	S41	-3224	249.5
707	S74	-2861	249.5	741	S40	-3235	349.5
708	S73	-2872	349.5	742	S39	-3246	149.5
709	S72	-2883	149.5	743	S38	-3257	249.5
710	S71	-2894	249.5	744	S37	-3268	349.5
711	S70	-2905	349.5	745	S36	-3279	149.5
712	S69	-2916	149.5	746	S35	-3290	249.5

PAD No.	PIN Name	X	Y
747	S34	-3301	349.5
748	S33	-3312	149.5
749	S32	-3323	249.5
750	S31	-3334	349.5
751	S30	-3345	149.5
752	S29	-3356	249.5
753	S28	-3367	349.5
754	S27	-3378	149.5
755	S26	-3389	249.5
756	S25	-3400	349.5
757	S24	-3411	149.5
758	S23	-3422	249.5
759	S22	-3433	349.5
760	S21	-3444	149.5
761	S20	-3455	249.5
762	S19	-3466	349.5
763	S18	-3477	149.5
764	S17	-3488	249.5
765	S16	-3499	349.5
766	S15	-3510	149.5
767	S14	-3521	249.5
768	S13	-3532	349.5
769	S12	-3543	149.5
770	S11	-3554	249.5
771	S10	-3565	349.5
772	S9	-3576	149.5
773	S8	-3587	249.5
774	S7	-3598	349.5
775	S6	-3609	149.5
776	S5	-3620	249.5
777	S4	-3631	349.5
778	S3	-3642	149.5
779	S2	-3653	249.5
780	S1	-3664	349.5

PAD No.	PIN Name	X	Y
781	DUMMY	-3675	149.5
782	DUMMY	-3686	249.5
783	DUMMY	-3697	349.5
784	DUMMY	-3708	149.5
785	DUMMY	-3719	249.5
786	DUMMY	-3730	349.5

5 BLOCK DIAGRAM



6 PIN DESCRIPTION

6.1 Power Supply Pins

Name	I/O	Description	Connect Pin
VDDI	I	- Power supply for I/O system. - VDDI must be lower than or equal to VDD.	VDDI
VDDA	I	- Power supply for analog and booster circuits. Input voltage level should be the same as VCI.	VCI
VDDM	I	- Power supply for MIPI circuits. Input voltage level should be the same as VCI.	VCI
VDDR	I	- Power supply for Gamma circuits . Input voltage level should be the same as VCI.	VCI
AGND	I	- System ground for analog system and booster circuit.	GND
AGNDR	I	- System ground for Gamma circuit.	GND
DGND	I	- System ground for I/O system and digital system.	GND
VPP	I	- Power supply for internal NVM. - Writing NVM needs external power supply voltage with 7.5V. - The current of Ivpp must be more than 10mA. - Leaves these pins open if not used.	External Power

6.2. Interface Logic Pins

Name	I/O	Description	Connect Pin
IMP	I	-The MCU interface mode select. -Only MIPI.	GND
RESXP	I	- This signal will reset the device and it must be applied to properly initialize the chip. - Signal is active low.	MCU
MIPI_CLK_P	I	-Positive polarity of low voltage differential clock signal.	MIPI
MIPI_CLK_N	I	-Negative polarity of low voltage differential clock signal.	MIPI
MIPI_DATA_P	I/O	-Positive polarity of low voltage differential data signal.	MIPI
MIPI_DATA_N	I/O	-Negative polarity of low voltage differential data signal.	MIPI
TEP	O	- Tearing effect output. - If not used, leave this pin open.	MCU

<table>
<tr>
<td>CSWP
DSWP</td>
<td>I</td>
<td>Differential clock polarity swap.
For MIPI interface.
<table>
<tr><th>CSWAP</th><th>DSWAP</th><th>CLK_P</th><th>CLK_N</th><th>D0_P</th><th>D0_N</th></tr>
<tr><td rowspan="2">0</td><td>0</td><td>CLK_N</td><td>CLK_P</td><td>D0_N</td><td>D0_P</td></tr>
<tr><td>1</td><td>CLK_N</td><td>CLK_P</td><td>D0_P</td><td>D0_N</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td>CLK_P</td><td>CLK_N</td><td>D0_N</td><td>D0_P</td></tr>
<tr><td>1</td><td>CLK_P</td><td>CLK_N</td><td>D0_P</td><td>D0_N</td></tr>
</table>
</td>
<td>VDDI/DGND</td>
</tr>
</table>

6.3. Driver Output Pins

Name	I/O	Description	Connect pin
S[1:600]	O	Source output voltage signals applied to liquid crystal.	LCD
GOUT[1:10]	O	Gate control signals and the swing voltage level is VGHO to VGLO.	LCD
VGH	O	- Power output pin for gate driver. - Leave open when not in use.	LCD
VGL	O	- Power output (Negative) pin for gate driver. - Leave open when not in use.	LCD
VGHS	O	Connect to VGH. - Leave open when not in use.	LCD

6.4. Test and Other Pins

Name	I/O	Description	Connect pin
Dummy	-	- These pins are dummy. - Leave the pin open.	OPEN
Dummyt	-	- These pins are dummy. - Leave the pin open.	OPEN
OSCP	I/O	- This pin is for testing. - Leave the pin open.	OPEN
HSTRIM	O	- This pin is for testing. - Leave the pin open.	OPEN
VCCM	O	-Used for monitoring. - Leave the pin open.	OPEN

VCCLP	O	Used for monitoring. - Leave the pin open.	OPEN
TSE[0:2]	I	- This pin is for testing - Leave the pin open.	OPEN
SVEE	O	-Used for monitoring. - Leave the pin open.	OPEN
SVDD	O	-Used for monitoring. - Leave the pin open.	OPEN
VCC	O	-Used for monitoring. - Leave the pin open.	OPEN
AVDD	O	-Power Pad for analog Circuit. - Leave the pin open.	OPEN
AVEE	O	-Power Pad for analog Circuit. - Leave the pin open.	OPEN
VAPP	O	-A power output of grayscale voltage. - Leave the pin open.	OPEN
VANP	O	-A power output (negative) of gray scale voltage. - Leave the pin open.	OPEN
VAG	O	- This pin is for testing. - Leave the pin open.	OPEN
V22P	O	-Used for monitoring. - Leave the pin open.	OPEN
ATS0	O	- This pin is for testing. - Leave the pin open.	OPEN
TEST[0:7]	O	- This pin is for testing - Leave the pin open.	OPEN

7. DRIVER ELECTRICAL CHARACTERISTICS

7.1. Absolute Operation Range

Item	Symbol	Range	Unit
Supply Voltage (Analog)	VCI	- 0.3 ~ +4.6	V
Supply Voltage (I/O)	VDDI	- 0.3 ~ +4.6	V
Supply Voltage (Logic)	VCC	-0.3 ~ +2	V
Driver Supply Voltage	VGH-VGL	-0.3 ~ +30.0	V
Logic Input Voltage Range	VIN	0.5 ~ VDDI + 0.5	V
Logic Output Voltage Range	VO	0.5 ~ VDDI + 0.5	V
Operating Temperature Range	TOPR	-30 ~ +85	℃
Storage Temperature Range	TSTG	-40 ~ +125	℃

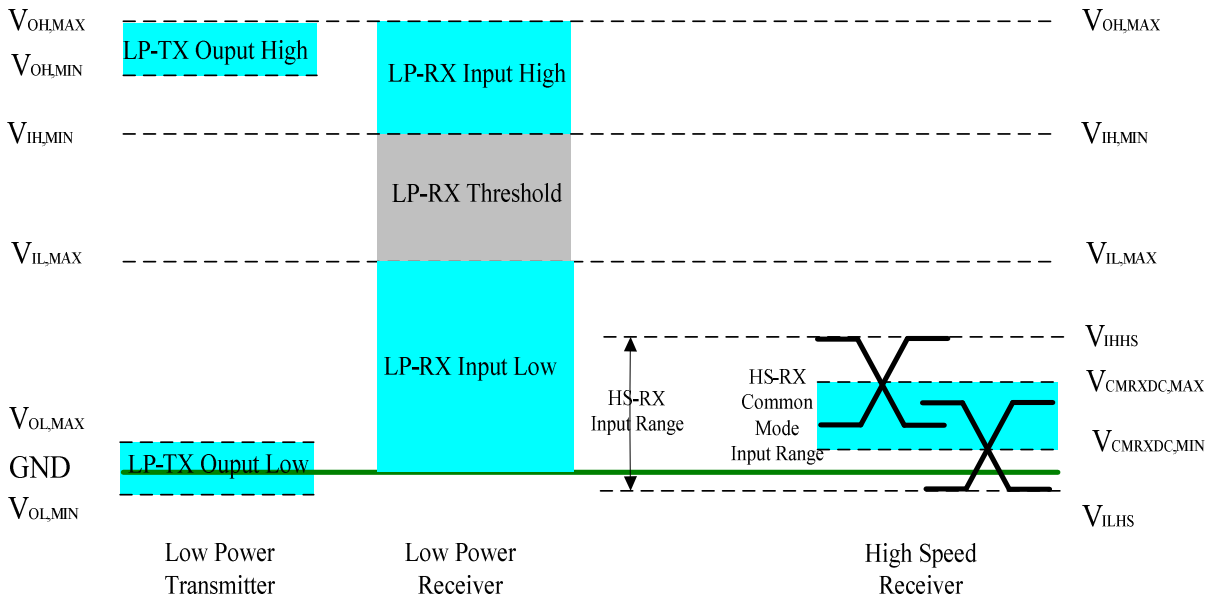
Absolute Operation Range

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

7.2. DC Characteristics

7.2.1. DC characteristics for MIPI DSI

- MIPI Signaling Voltage Levels



- MIPI DC characteristics

Parameter	Symbol	Specification			Unit
		MIN	TYP	MAX	
Operation Voltage for MIPI Receiver					
Low power mode operating voltage	VLPH	1.1	1.2	1.3	V
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	V ILHS	-40	-	-	mV
Single-ended input high voltage	V IHHS	-	-	460	mV
Common-mode voltage	VCMRXDC	70	-	330	mV
Differential input impedance	Z ID	80	100	125	ohm
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	VI	-5 0	-	1350	mV
Logic 0 input threshold	VIL	0	-	550	mV
Logic 1 input threshold	VIH	88 0	-	-	mV
Output low level	VOL	-5 0	-	50	mV
Output high level	VOH	1.1	1.2	1.3	V

7.2.2. DC Characteristics for Panel Driving

Parameter	Symbol	Condition	Specification			Unit	Related Pins
			MIN.	TYP.	MAX.		
Power & Operation Voltage							
System Voltage	VDD / VDDA	Operating voltage	2.5	2.75	3.3	V	-
Interface Operation Voltage	VDDI	I/O Supply Voltage	1.65	1.8	3.3	V	-
Gate Driver High Voltage	VGH	-	12.6	-	15.5	V	-
Gate Driver Low Voltage	VGL	-	-11.8	-	-8.3	V	-
Gate Driver Supply Voltage	-	| VGH-VGL |	-	-	27.3	V	-
Input / Output							
Logic-High Input Voltage	VIH	-	0.7VDDI	-	VDDI	V	Note 1
Logic-Low Input Voltage	VIL	-	VSS	-	0.3VDDI	V	Note 1

Differential Input High Threshold Voltage	VIT+	-	-	0	50	mV	MIPI_CLK, MIPI_DATA
Differential Input Low Threshold Voltage	VIT-	-	-50	0	-	mV	
Single-ended Receiver Input Operation Voltage Range	VIR	-	0.5	-	1.2	V	
Logic-High Output Voltage	VOH	IOH = -1.0mA	0.8VDDI	-	VDDI	V	Note 1
Logic-Low Output Voltage	VOL	IOL = +1.0mA	VSS	-	0.2VDDI	V	Note 1
Logic-High Input Current	IIH	VIN = VDDI	-	-	1	uA	Note 1
Logic-Low Input Current	IIL	VIN = VSS	-1	-	-	uA	Note 1
Input Leakage Current	ILI	IOH = -1.0mA	-0.1	-	+0.1	uA	Note 1
VCOM Voltage							
VCOM Voltage	VCOM	-	-	VSS	-	V	-
Source Driver							
Gamma Reference Voltage(Positive)	VAP	-	4.45	-	6.4	V	-
Gamma Reference Voltage(Negative)	VAN	-	-4.6	-	-2.65	-	-
Source Output Settling Time	Tr	Below with 99% precision	-	-	20	us	Note 2
Output Offset Voltage	VOFFSET	-	-	-	35	mV	Note 3

Basic DC Characteristics

Notes:

1. TA= -30 to 85℃.

2. The max. value is between measured point of source output and gamma setting value.

7.3. Power Consumption

Ta=25℃, Frame rate = 30Hz, Registers setting are IC default setting.

Operation Mode	Image	Current Consumption			
		Typical		Maximum	
		IDDI (mA)	IDD (mA)	IDDI (mA)	IDD (mA)
Normal Mode	Note	1.97	6.03	0.078	8.12
Slpin Mode	Note	0	0.037	0	0.055
Stand by Mode	Note	0	0	0	0

Notes:

1. Color Picture.

2. The Current Consumption is DC characteristics of ST7797.

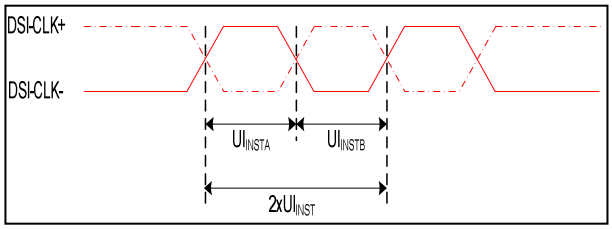
3. Typical: VDDI=1.8V, VCI=2.8V; Maximum: VDDI=3.3V, VCI=3.3V

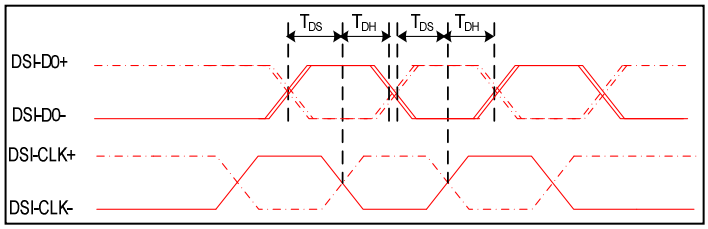
4. Maximum can not be used VCCM/VCC Bypass

7.4. MIPI Interface Characteristics

7.4.1. High Speed Mode

- Clock Channel Timing

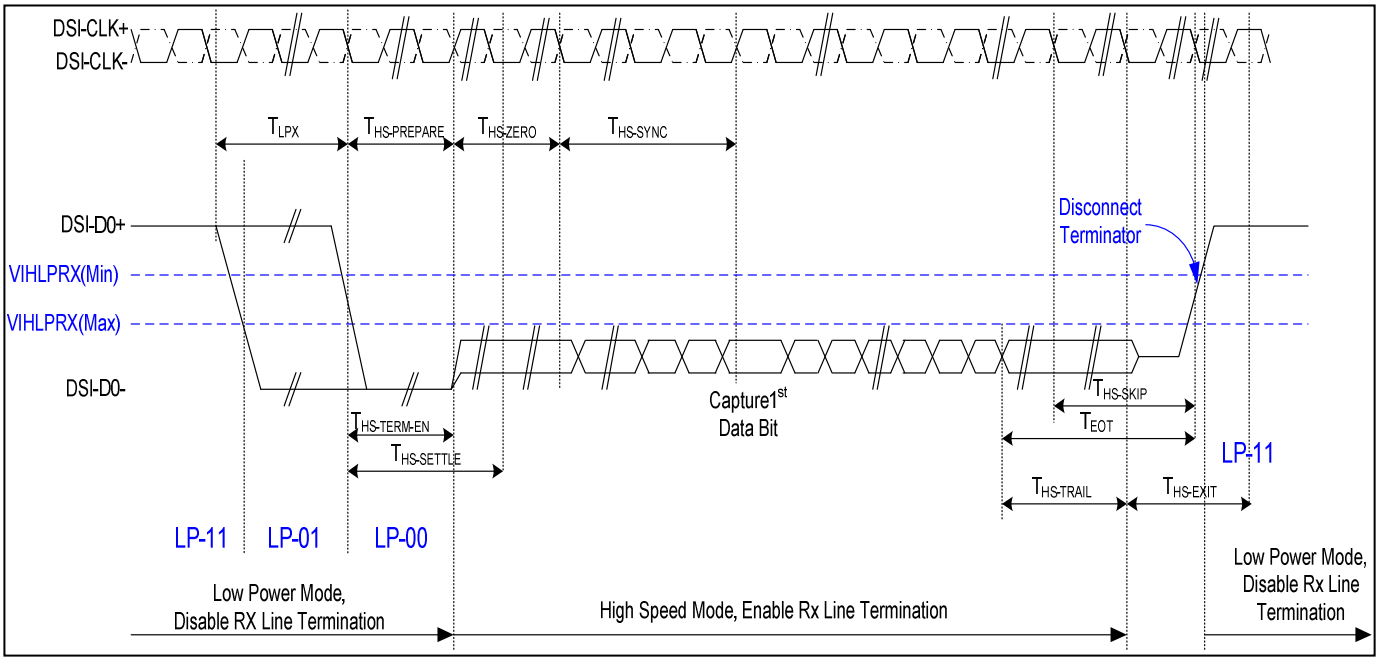




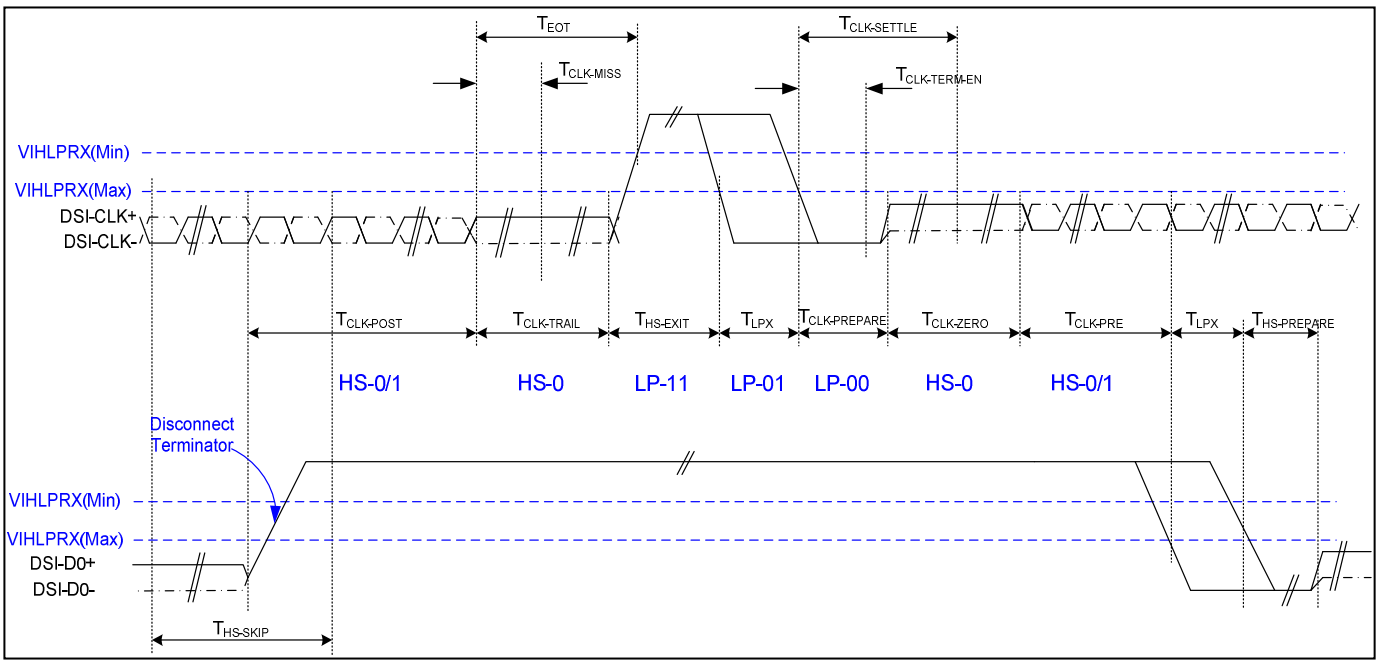
- Timing Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	4	25	ns	-
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	2	12.5	ns	$UI = UI_{INSTA} = UI_{INSTB}$
DSI-Dn+/-	tDS	Data to clock setup time	0.15	-	UI	-
DSI-Dn+/-	tDH	Data to clock hold time	0.15	-	UI	-

- Data Transmission



Data lanes-Low Power Mode to/from High Speed Mode Timing

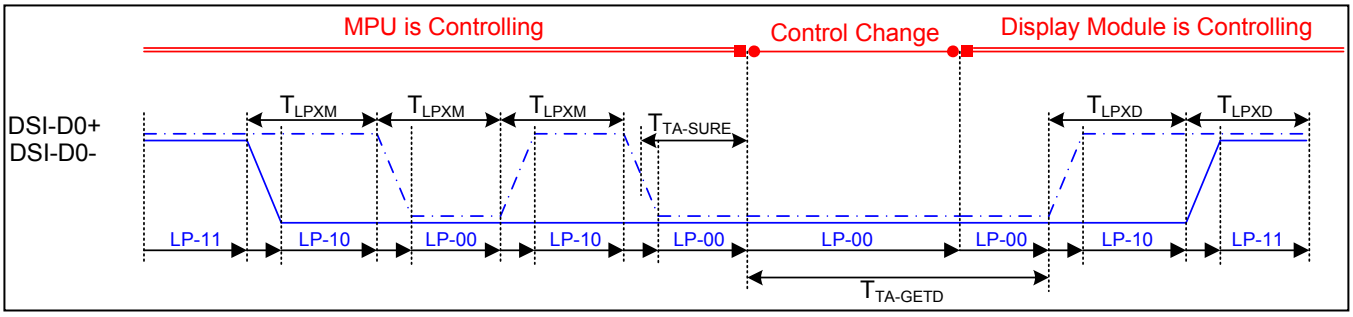


Clock lanes- High Speed Mode to/from Low Power Mode Timing

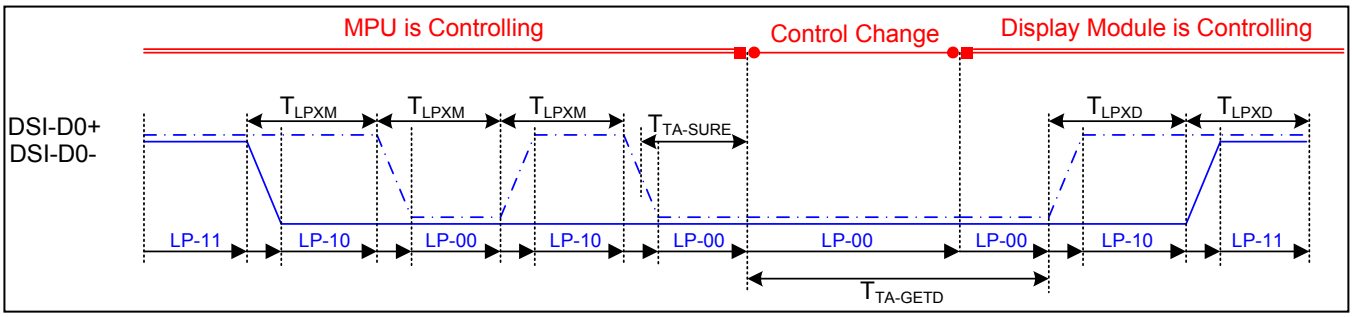
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4UI	85+6UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+52UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	--	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105ns+12UI	ns	Input

Mipi Interface- High Speed Mode Timing Characteristics

7.4.2. Bus Turnaround Procedure



Bus Turnaround (BTA) from display module to MPU Timing



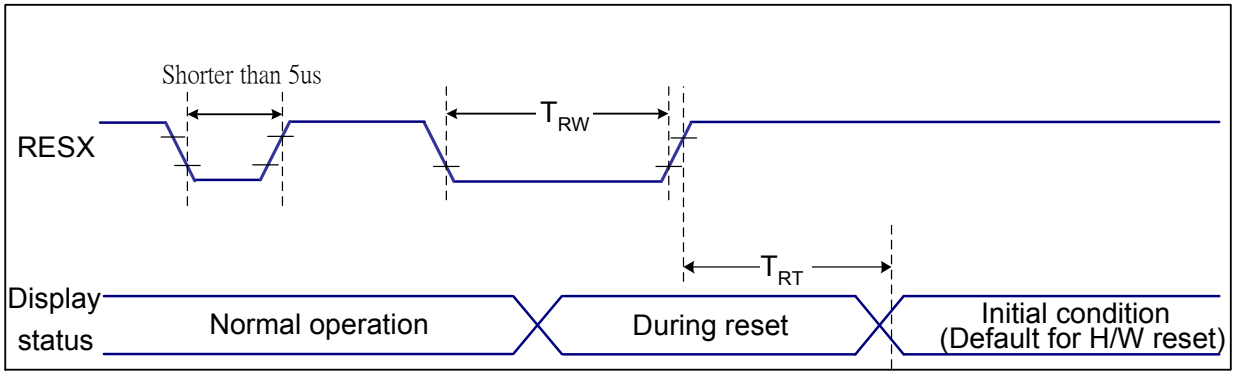
Bus Turnaround (BTA) from MPU to display module Timing

VDDI=1.8V,VCI=2.8V, AGND=DGND=AGNDR=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5xT_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4xT_{LPXD}$		ns	Output

MIPI Interface BTA ModeTiming Characteristics

7.5. Rest Timing



VDDI=1.8V,VCI=2.8V, AGND=DGND=AGNDR=0V, Ta=25℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
			-	120 (Note 1, 6, 7)	ms

Notes:

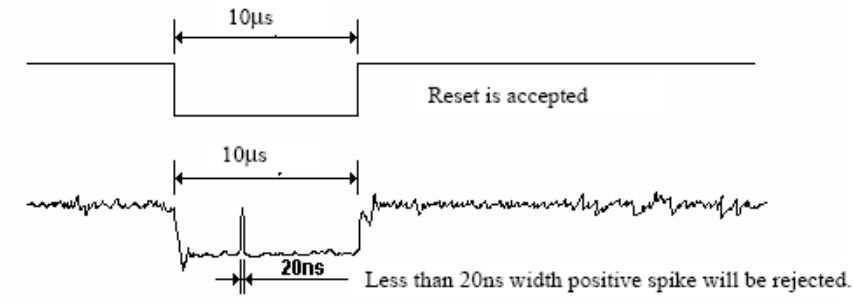
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. MIPI FUNCTION DESCRIPTION

8.1. MIPI DSI Interface

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

Typically, a peripheral is capable of Command Mode operation or Video Mode operation. Some Video Mode display modules also include a simplified form of Command Mode operation in which the display module may refresh its screen from a reduced-size, or partial, frame buffer, and the interface (DSI) to the host processor may be shut down to reduce power consumption.

Command Mode refers to operation in which transactions primarily take the form of sending commands to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers. The host processor indirectly controls activity at the peripheral by sending commands, parameters to the display controller.

The host processor can also read display module status information. Command Mode operation requires a bidirectional interface.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. Some Video Mode architectures may include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to be shut down to reduce power consumption. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

Configuration:

Lane Pair	MCU (Master) Display Module (Slave)
Clock Lane	Unidirectional Lane ■ Clock Only ■ Escape Mode(ULPS Only)
Data Lane 0	Bi-directional Lane ■ Forward High-Speed ■ Bi-directional Escape Mode ■ Bi-directional LPDT

8.2. Display Serial Interface (DSI)

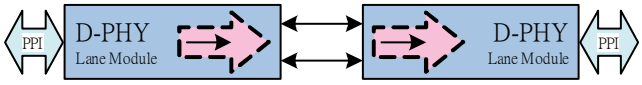
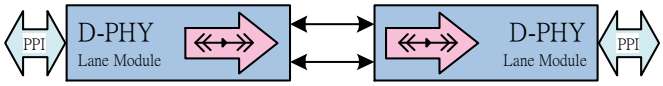
8.2.1. General Description

The communication can be separated 2 different levels between the MCU and the display module:

- Interface Level : Low level communication
- Packet level : High level communication

8.2.2. Interface level communication

The display module uses data and clock lane differential pairs for DSI . Both clock lane and data lane0 can be driven Low Power (LP) or High Speed (HS) mode.

	Lane support mode	
Clock Lane	Unidirectional lane High-Speed Clock only Simplified Escape Mode (ULPS Only)	
Data Lane0	Bi-directional lane Forward high-speed only Bi-directional Escape Mode Bi-direction LPDT	

The interface clock Lane types and support mode

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode. High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State Code	Line DC voltage Levels		High Speed(HS)	Low-Power(LP)	
	Dn+ Line	Dn- Line	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

High Speed and Low-Power Lane Pair State Descriptions

Notes:

1. Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.

2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

8.2.3. DSI-CLK Lanes

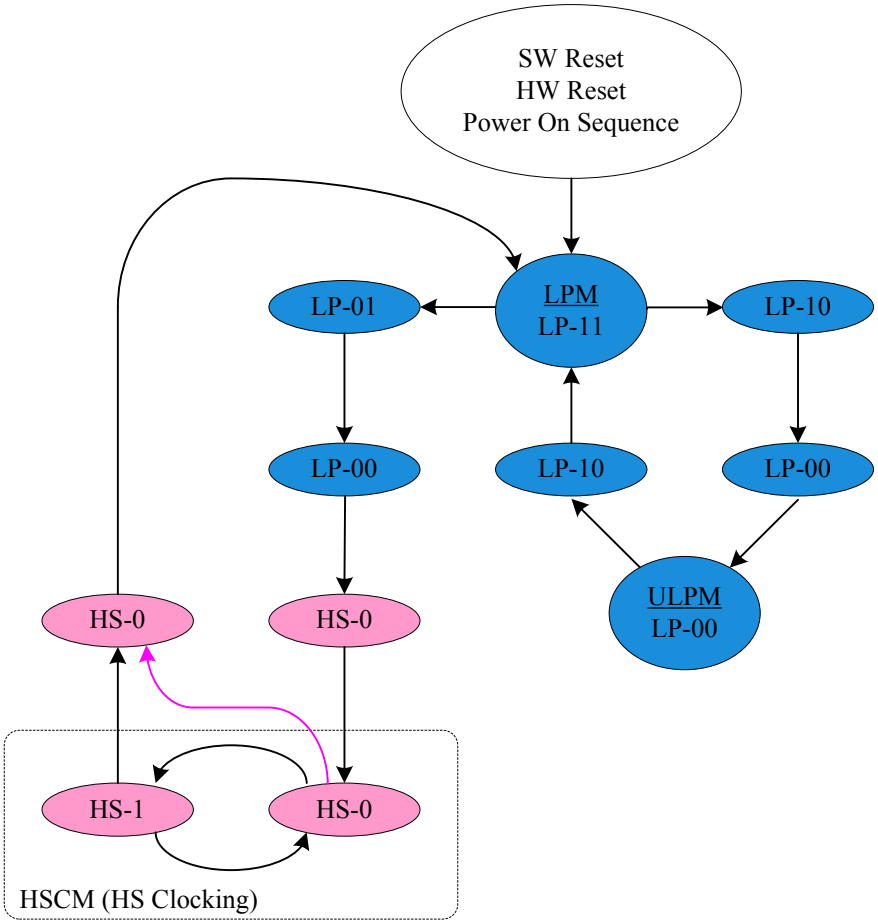
DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM LP-11), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM).

Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode(LPM) or Ultra Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.



Clock Lanes Power Modes

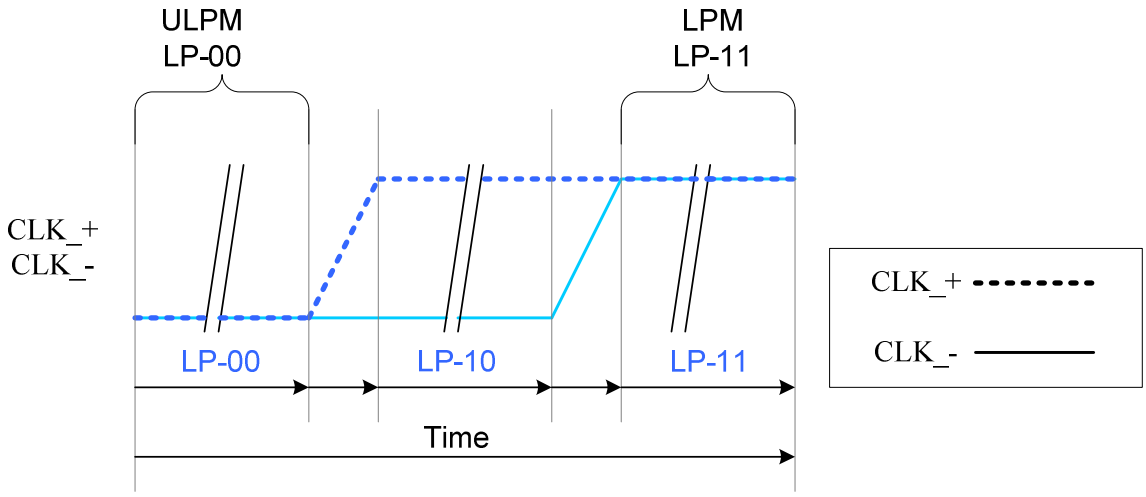
8.2.4. Low Power Mode

DSI-CLK+/- lanes can be driven to the Low Power Mode(LMP),when DSI-CLK lanes are entering LP-11 State Code , in three different ways:

After SW Reset,HW Reset or Power On Sequence=>LP-11

After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM,LP-00 State Code)=>LP10=>LP-11(LPM).

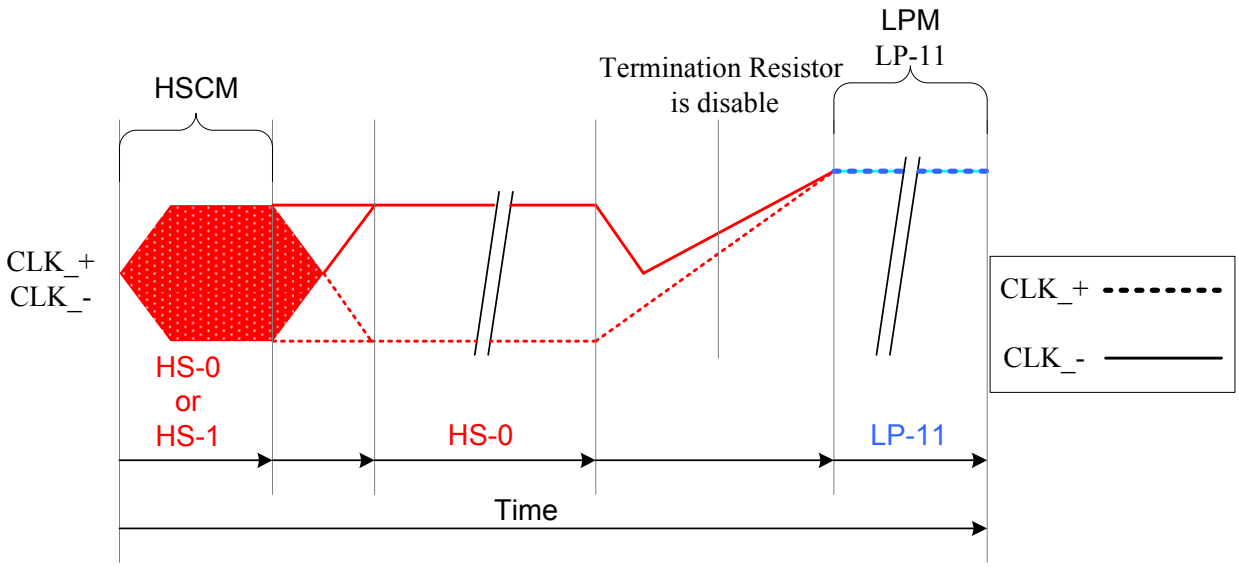
This sequence is illustrated below.



From ULPM to LPM

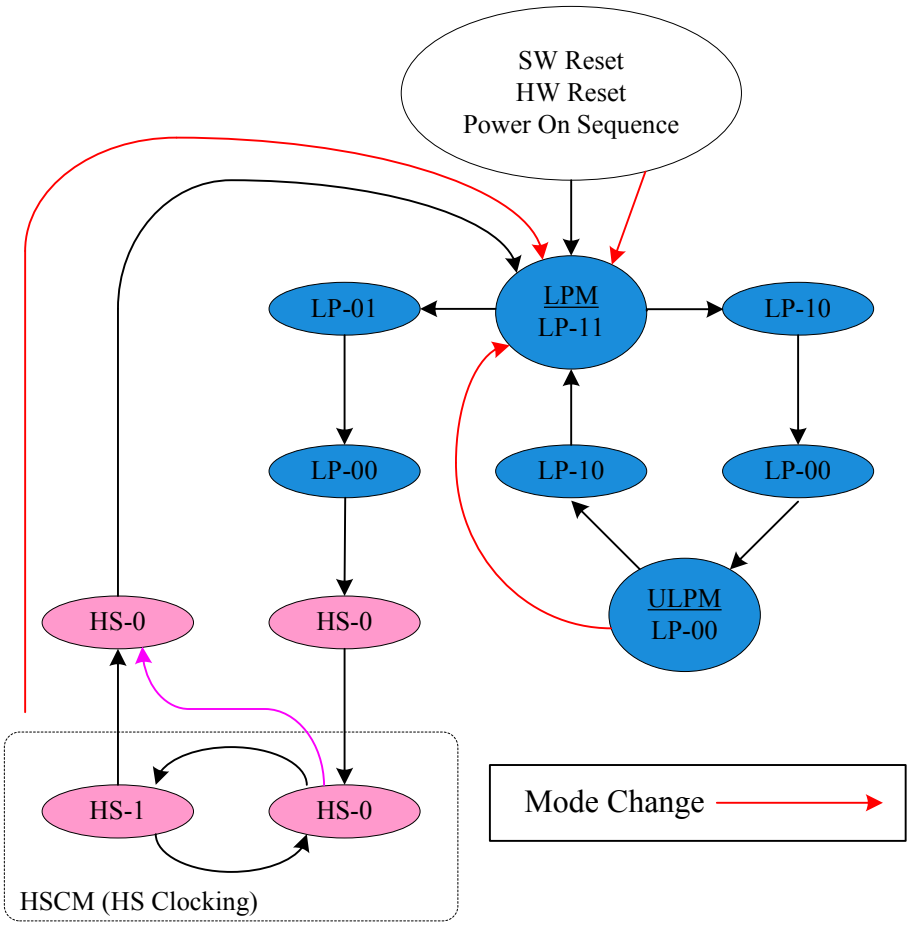
After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM).

This sequence is illustrated below.



From HSCM to LPM

All three mode changes are illustrated a flow chart below.



All three mode changes to LPM

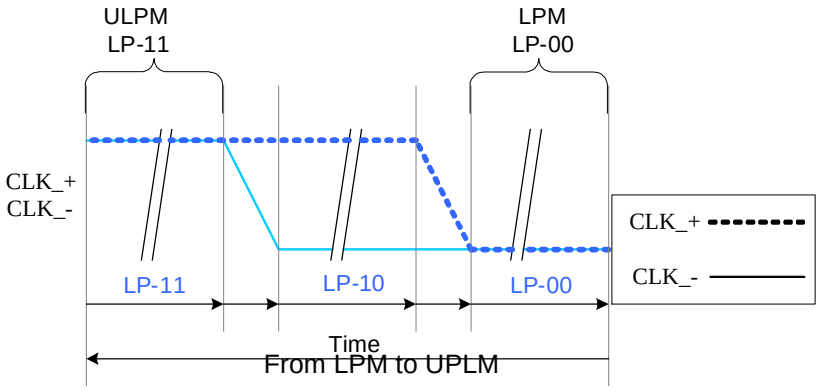
8.2.5. Ultra Low Power Mode

DSI-CLK+/- lanes can be driven to the Ultra Low power Mode (ULPM), when DSI-CLK lanes are entering LP-00

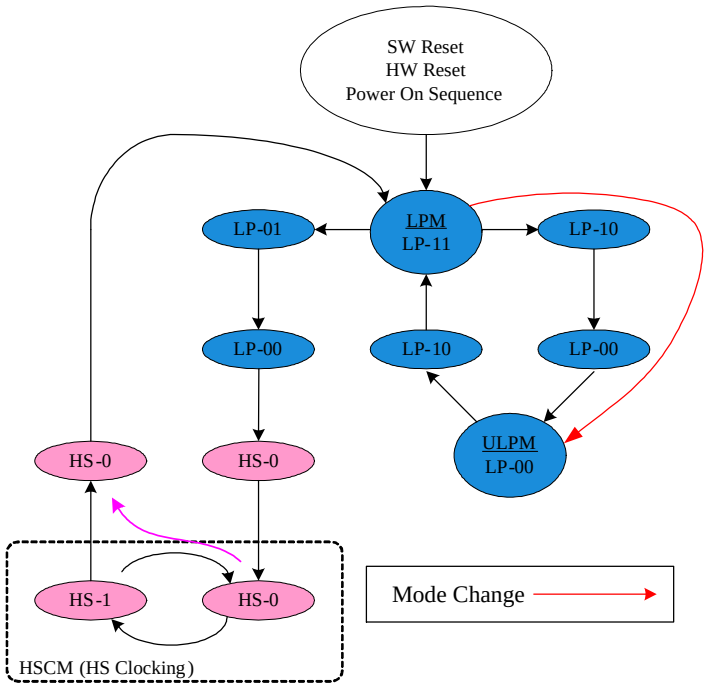
State Code.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-10 =>LP-00(ULPM).

This sequence is illustrated below.



The mode change is also illustrated below:



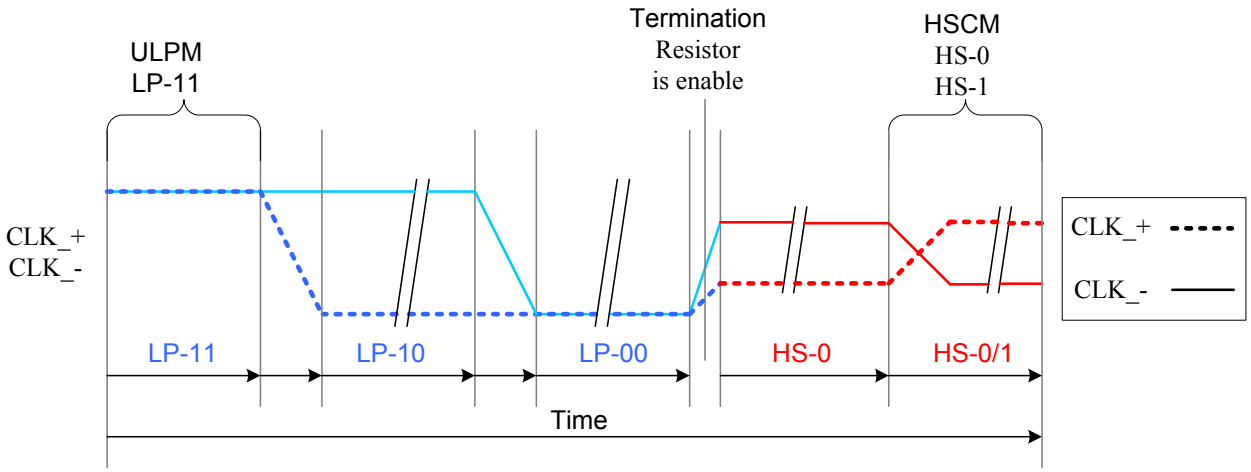
The mode change from LPM to UPLM

8.2.6. High-speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

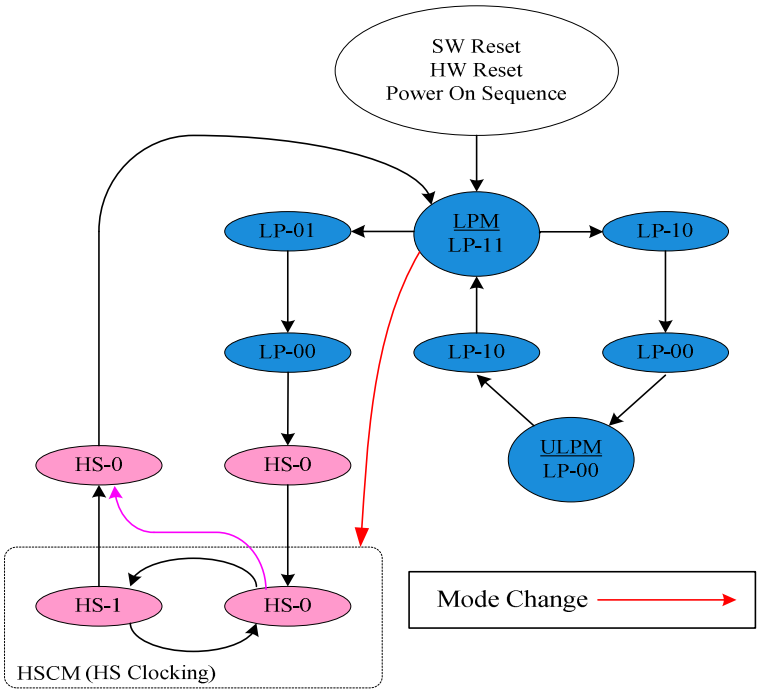
The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM).

This sequence is illustrated below.



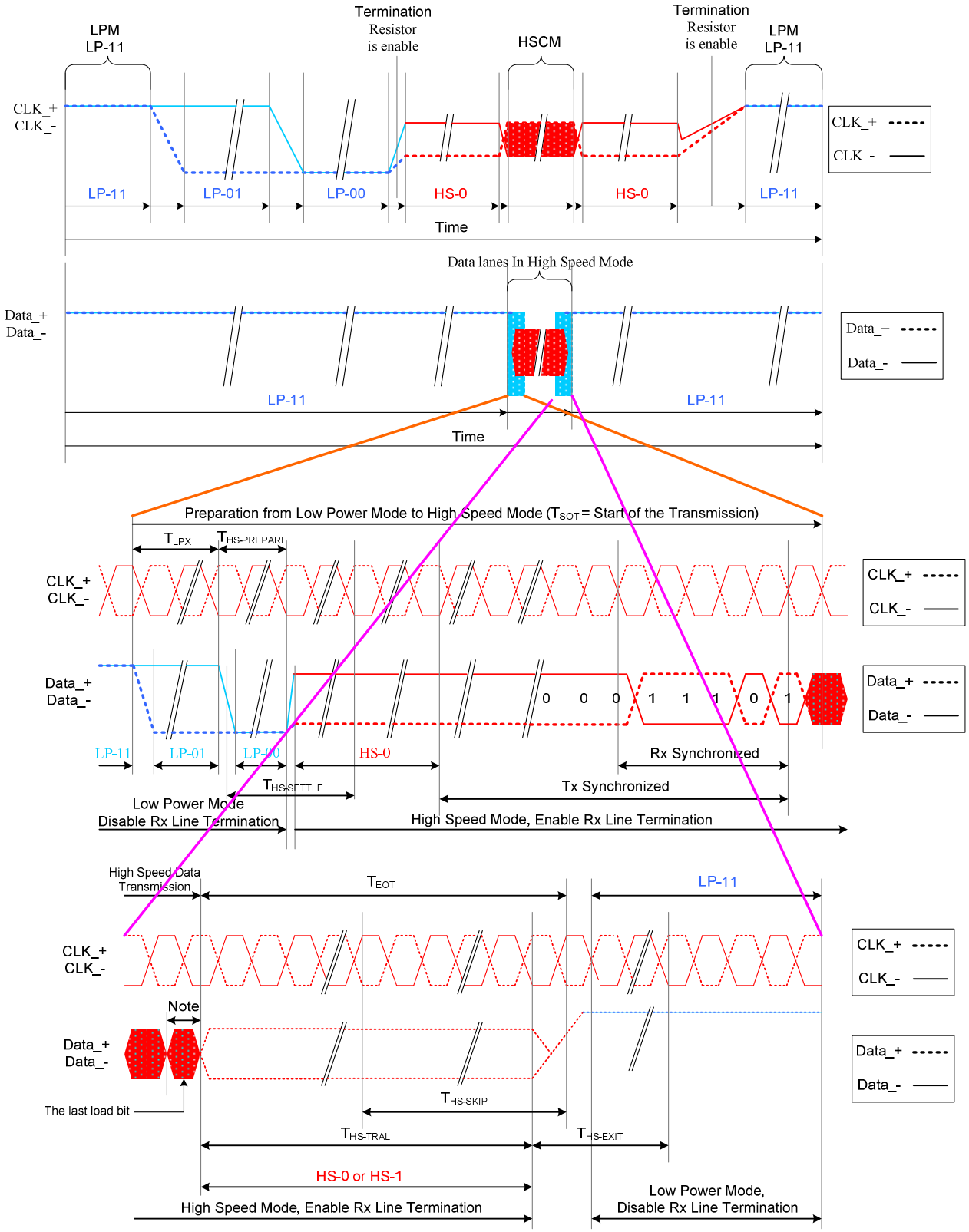
From LPM to HSCM

The mode change is also illustrated below:



Mode Change from LPM to HSCM on the Flow Chart

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped.



High Speed Clock Burst

8.2.7. DSI-DATA LANES

8.2.7.1 GENERAL

DSI-D0+/- Data Lanes can be driven in different modes which are:

• Escape Mode (Only DSI-D0+/- data lanes are used)

• High-Speed Data Transmission (DSI-D1+/- and DSI-D0+/- data lanes are used)

• Bus Turnaround Request (Only DSI-D0+/- data lanes are used)

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11=>LP-10=>LP-00=>LP-01=>LP-00	LP-00=>LP-10=>LP11(Mark1)
High-Speed Data Transmission	LP-11=>LP-01=>LP-00=>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11=>LP-10=>LP-00=>LP-10=>LP-00	High-Z

Notes:

1. Only DSI-D0+/- data lanes are used.

2. More information on section "Bus Turnaround (BTA)"

8.2.7.2 ESCAPE MODE

Data lanes (DSI-D0+/-) can be used in different Escape Modes when data lanes are in Low Power (LP) mode. These Escape Modes are used to:

• Send "Low-Power Data Transmission" (LPDT) e.g. from the MCU to the display module

• Drive data lanes to "Ultra-Low Power State" (ULPS)

• Indicate "Remote Application Reset" (RAR), which is reset the display module

• Indicate "Tearing Effect" (TEE), which is used for a TE trigger event from the display module to the MCU

• Indicate "Acknowledge" (ACK), which is used for a non-error event from the display module to the MCU

The basic sequence of the Escape Mode is as follow

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

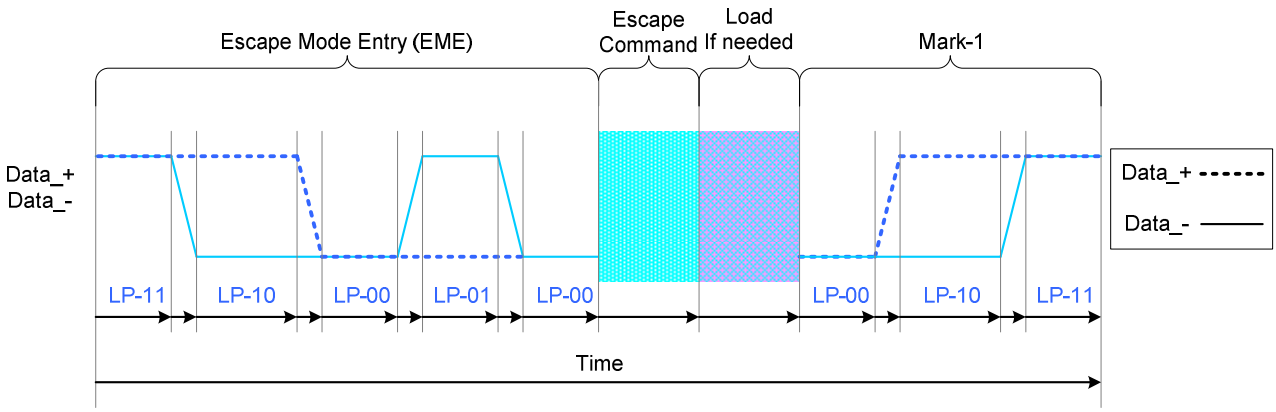
• Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0- = 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.

• A load if it is needed

• Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11

• End: LP-11

This basic construction is illustrated below:



General Escape Mode Sequence

The number of the different Escape Commands (EC) is eight. These eight different escape commands (EC) can be divided 2 different groups: Mode or Trigger. The MCU is informing to the display module that it is controlling data lanes (DSI-D0+/-) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the low power mode. The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it. Escape commands are defined on the next table.

This basic construction is illustrated below:

Escape command	Command Type Mode / Trigger	Entry command Pattern (First Last Bit Transmitted)
Low-Power Data	Mode	1110 0001 b
Ultra-Low Power Mode	Mode	0001 1110 b
Undefined-1, Note	Mode	1001 1111 b
Undefined-2, Note	Mode	1101 1110 b
Remote Application Reset	Trigger	0110 0010 b
Tearing Effect	Trigger	0101 1101 b
Acknowledge	Trigger	0010 0001 b
Uknown-5, Note	Trigger	1010 0000 b

Note: This Escape command support has not been implemented on the display module.

- Low-Power Data Transmission(LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU. The Low Power Data Transmission (LPDT) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)

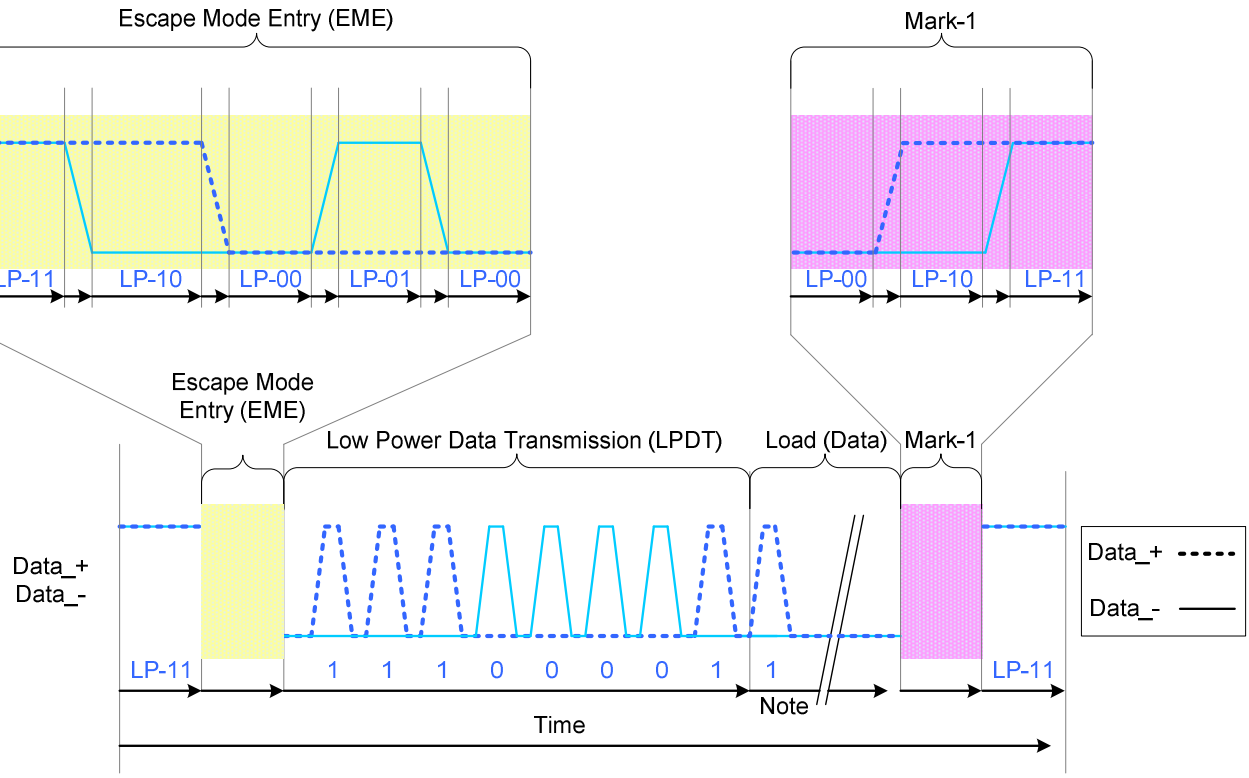
• Load (Data): One or more bytes (8 bits)

Data lanes are in pause mode when data lanes are stopped (Bothe lanes are low) between bytes

• Mark-1: LP-00 =>LP-10 =>LP-11

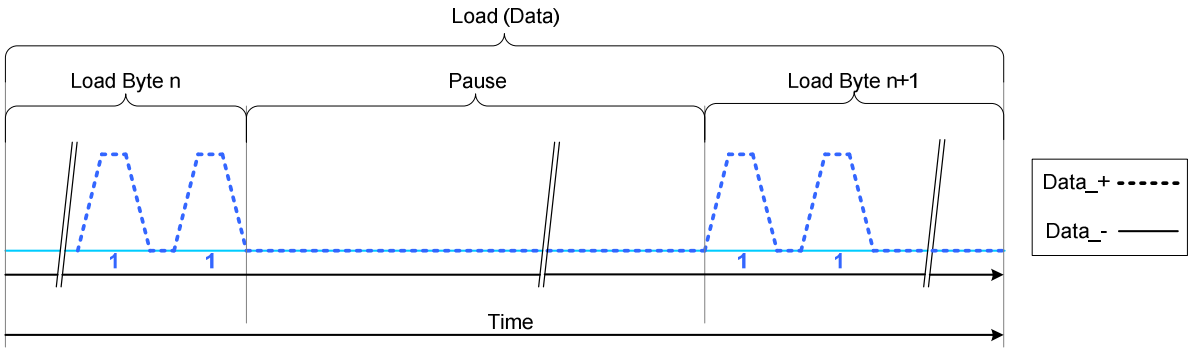
• End: LP-11

This sequence is illustrated for reference purposes below:



Note : Load (Data) is presenting that the first bit is logical “1” in this Exsample

Low-Power Data Transmission (LPDT)



Pause (Example)

- Ultra-Low Power State(ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape

Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

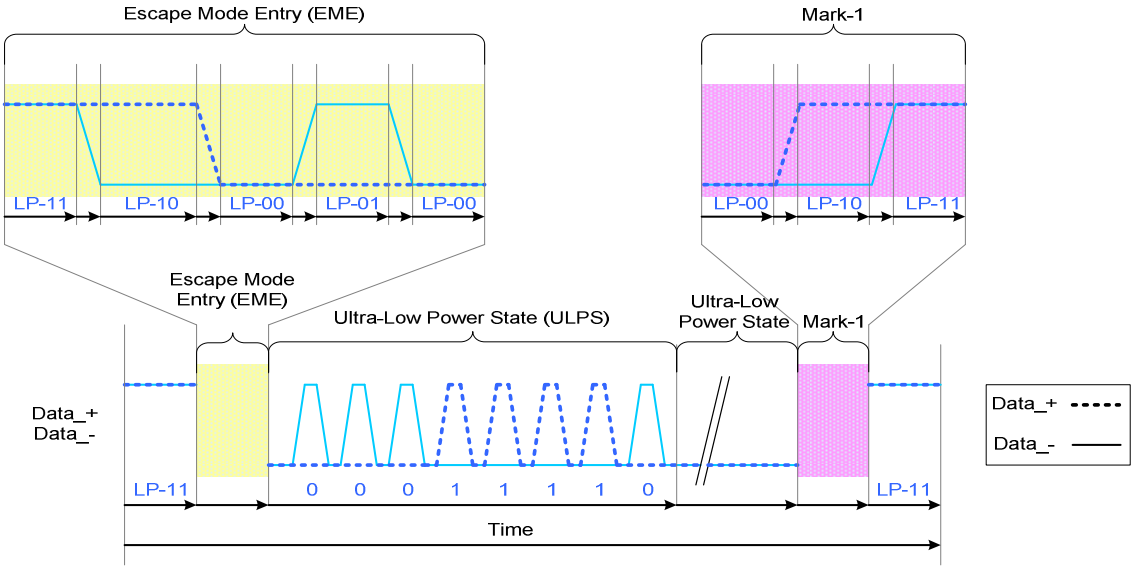
• Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)

• Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:



Ultra-Low Power State (ULPS)

- Remote Applicaition Reset(RAP)

The MCU can inform to the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

• Start: LP-11

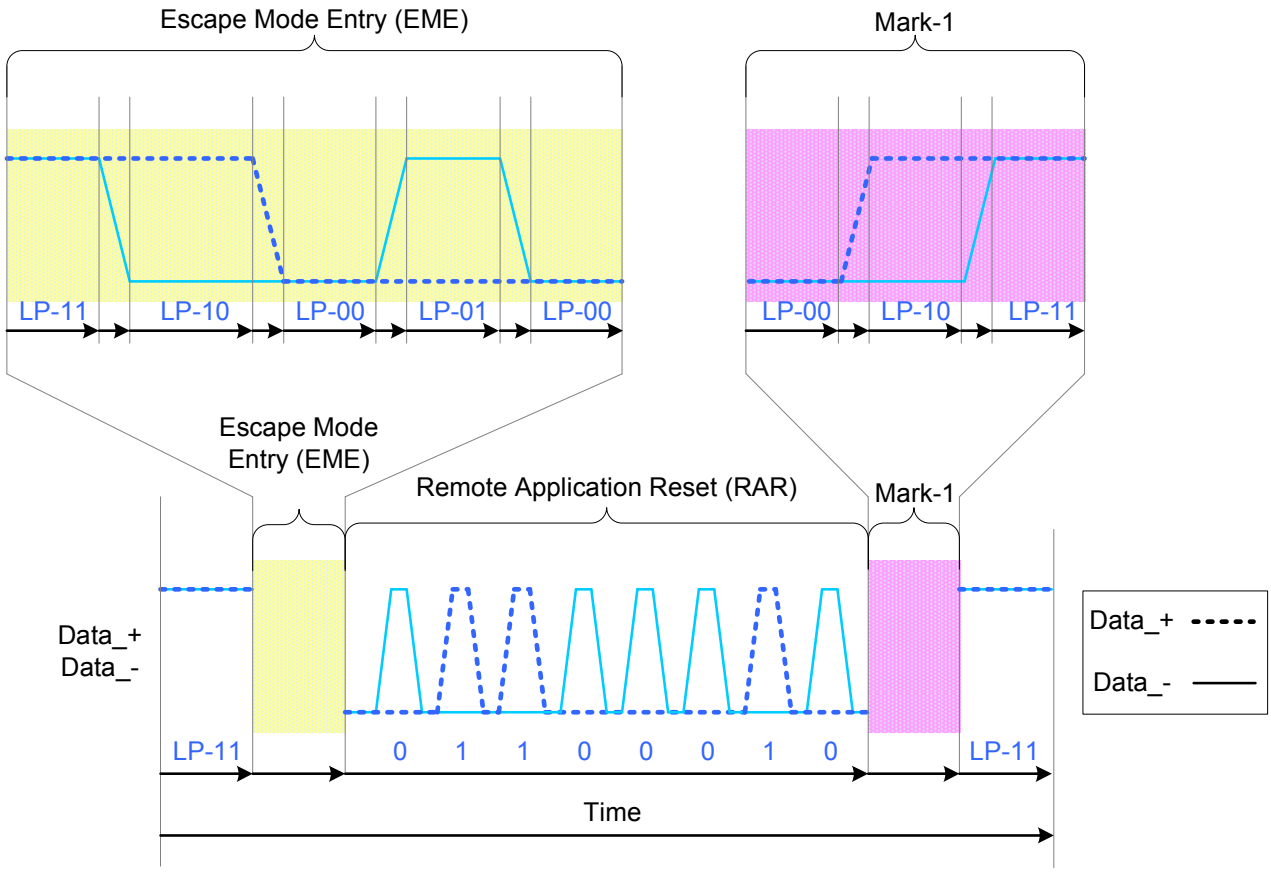
• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:



Remote Application Reset (RAR)

- Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

• Start: LP-11

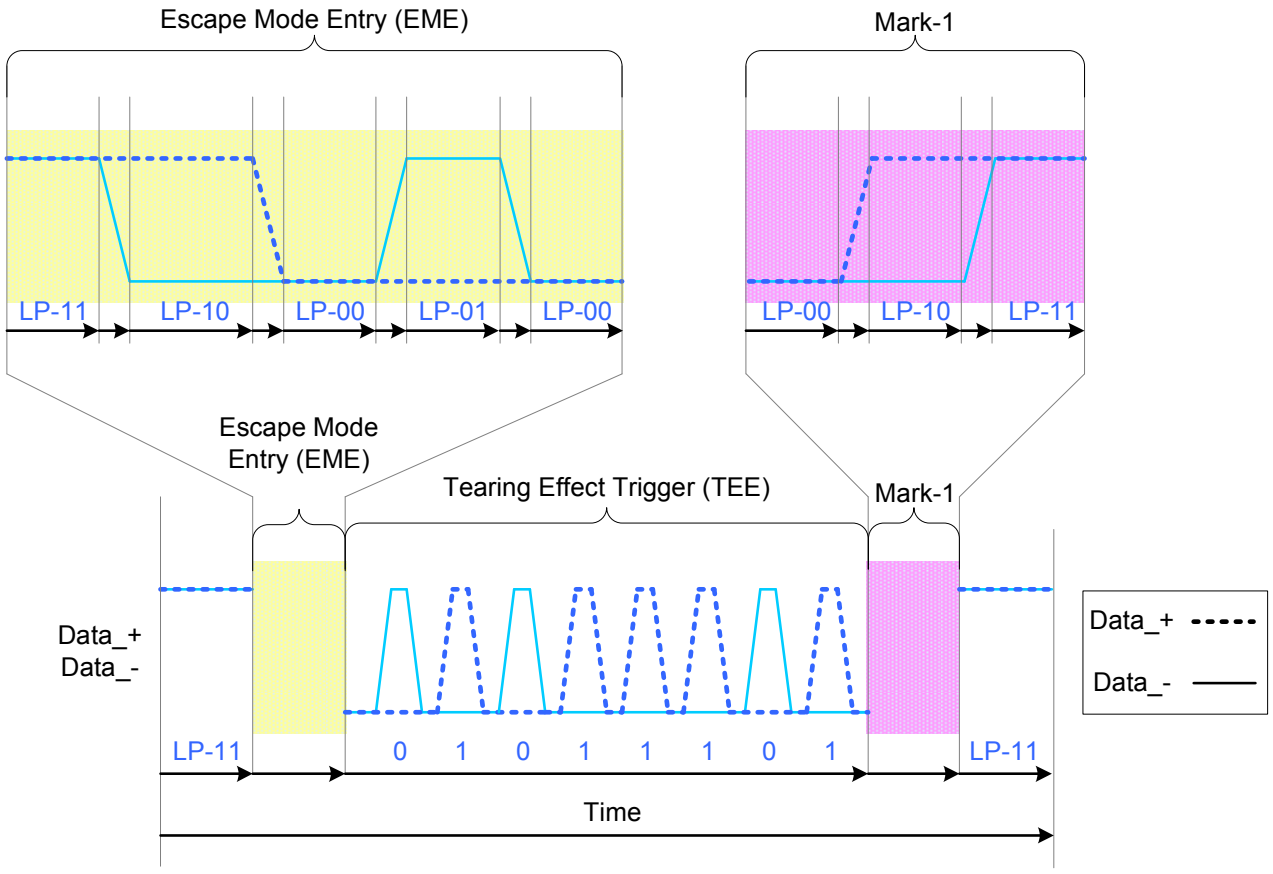
• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:



Tearing Effect (TEE)

Note: Tearing Effect (TEE) can not be used in MIPI Video Mode

- Acknowledge(ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) is using a following sequence:

• Start: LP-11

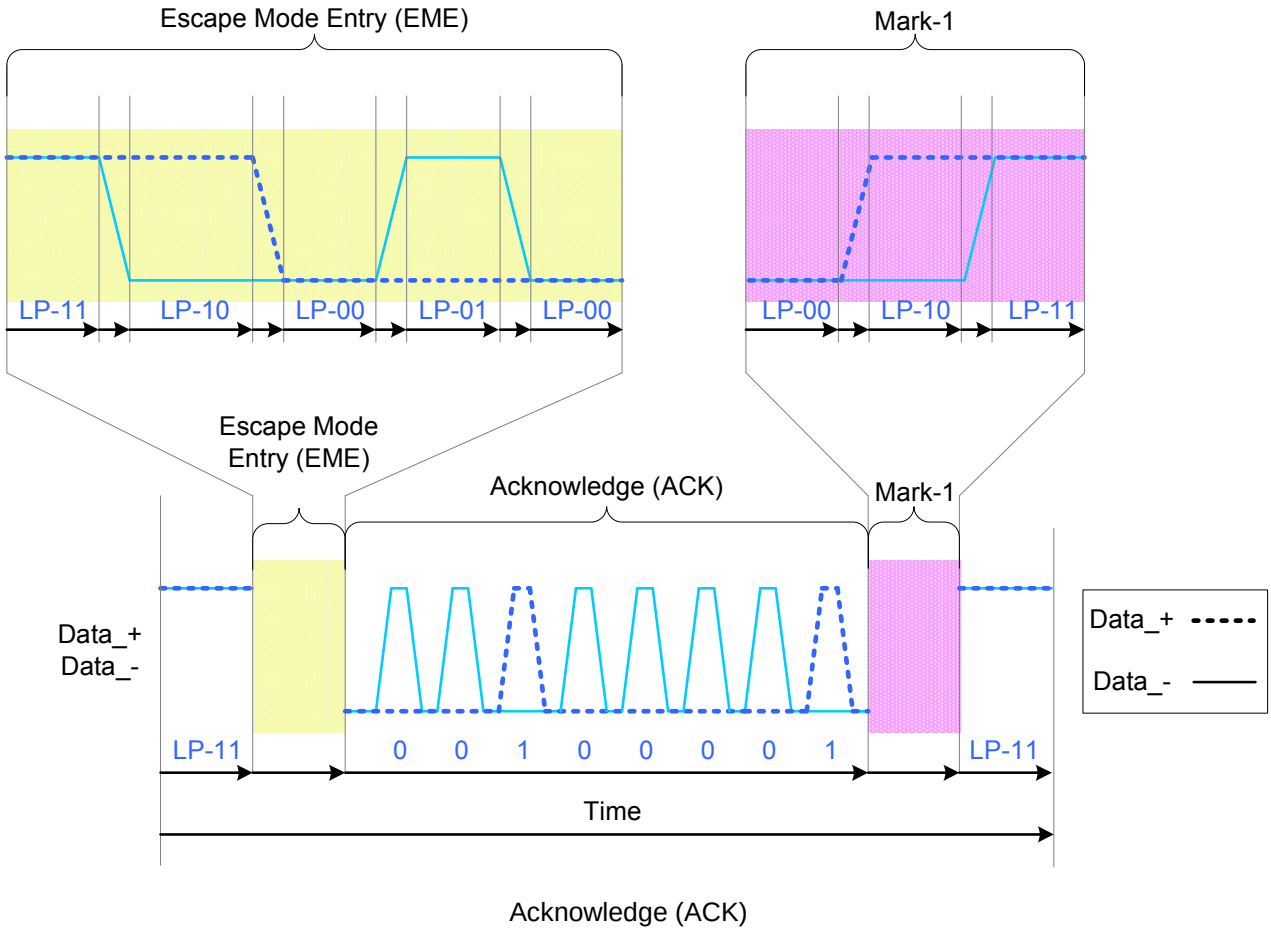
• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:



Acknowledge (ACK)

8.2.8. High Speed Data Transmisson(HSDP)

- Entering High-Speed Data Transmission (T_{SOT} of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU.

Data lanes of the display module are entering (TSOT) in the High-Speed Data Transmission (HSDT) as follows

• Start: LP-11

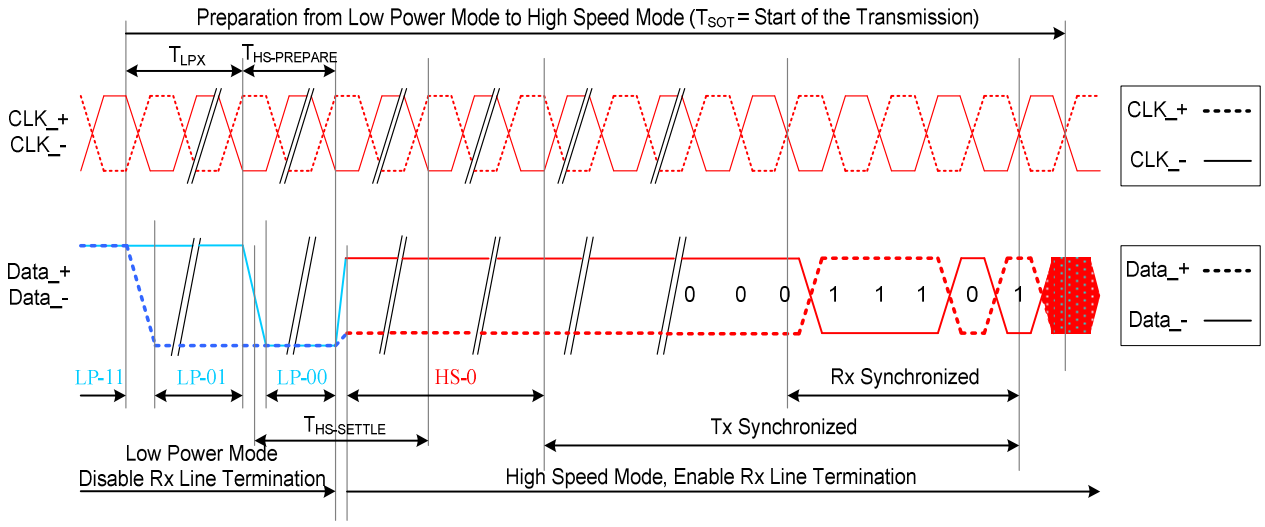
• HS-Request: LP-01

• HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)

• Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)

• End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (TSOT of HSDT) sequence is illustrated below



Entering High-Speed Data transmission (T_{SOT} of HSDT)

- Leaving High-Speed Data Transmission (T_{SOT} of HSDT)

The display module is leaving the High-Speed Data Transmission (TEOT of HSDT) when Clock lanes DSI-CLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes are in LP-11 mode.

Data lanes of the display module are leaving from the High-Speed Data Transmission (TEOT of HSDT) as follows

• Start: High-Speed Data Transmission (HSDT)

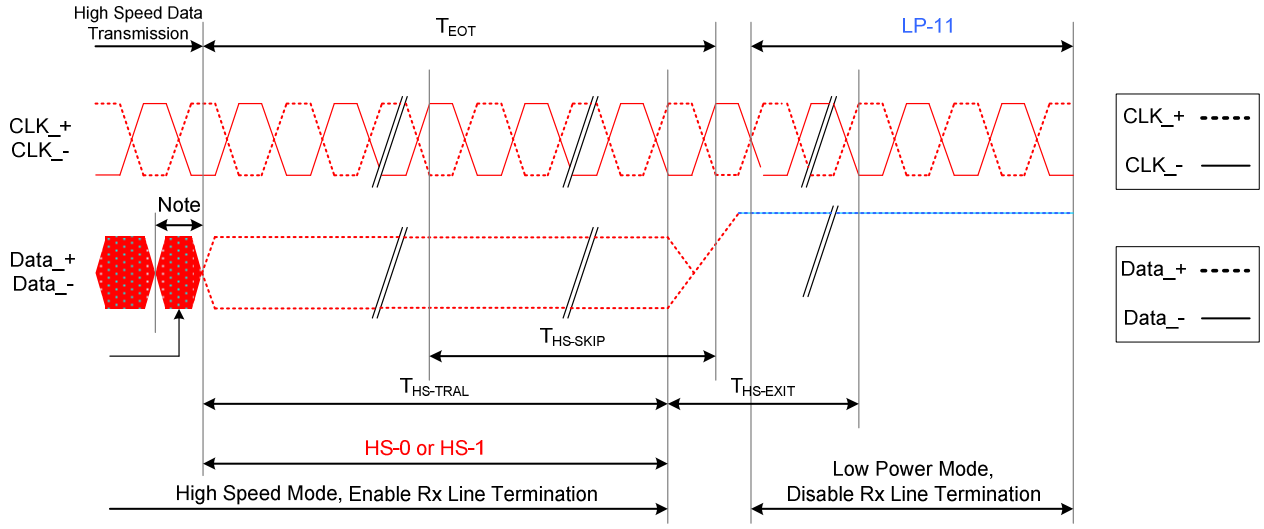
• Stops High-Speed Data Transmission

• MCU changes to HS-1, if the last load bit is HS-0

• MCU changes to HS-0, if the last load bit is HS-1

• End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (TEOT of HSDT) sequence is illustrated below



Levaving High-Speed data Transmission (T_{EOT} of HSDT)

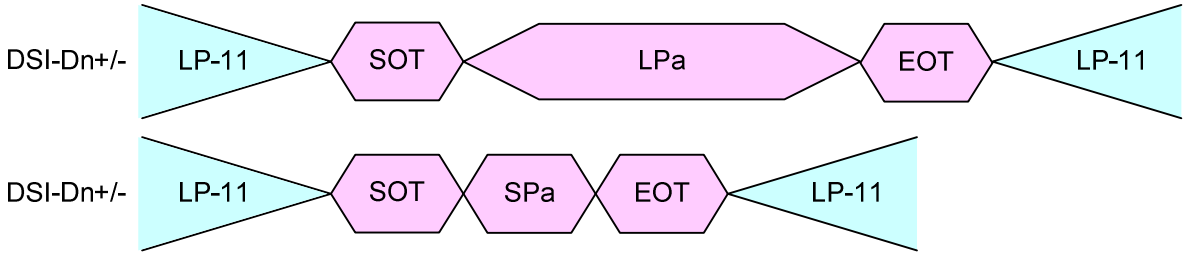
- Burst of the High-Speed Data Transmission(HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets.

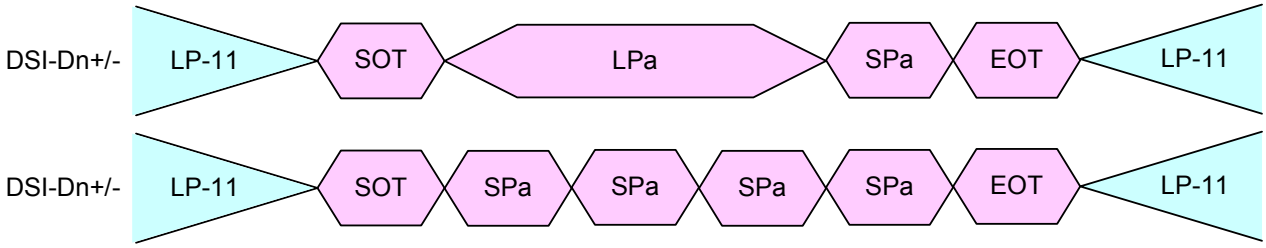
These data packets can be Long (LPa) or Short (SPa) packets.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

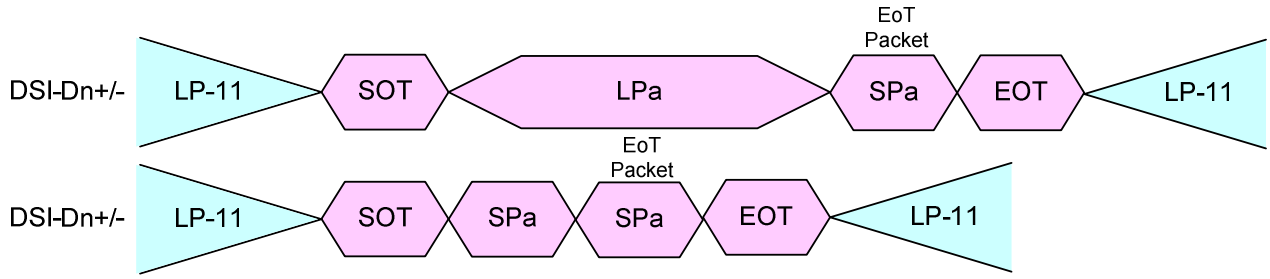
Single Packet in High Speed Data Transmission



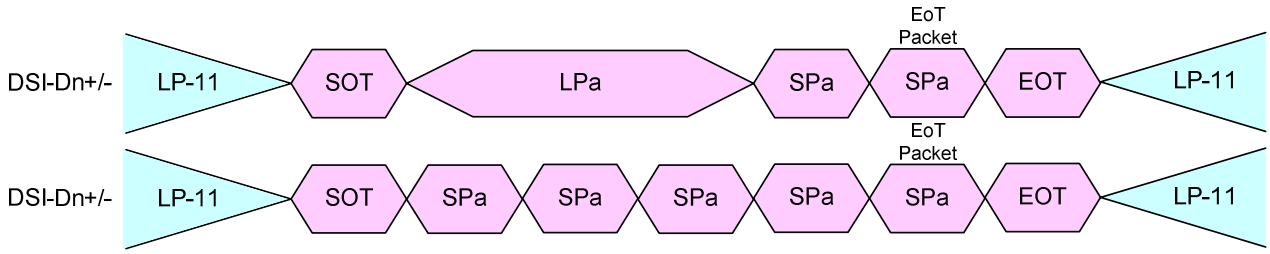
Multiple Packets in High Speed Data Transmission



Single Packet in High Speed Data Transmission



Multiple Packets in High Speed Data Transmission



Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Data lanes are'1's (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

- Bus Turnaround(BTA)

The MCU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module.

The MCU or display module are using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follow.

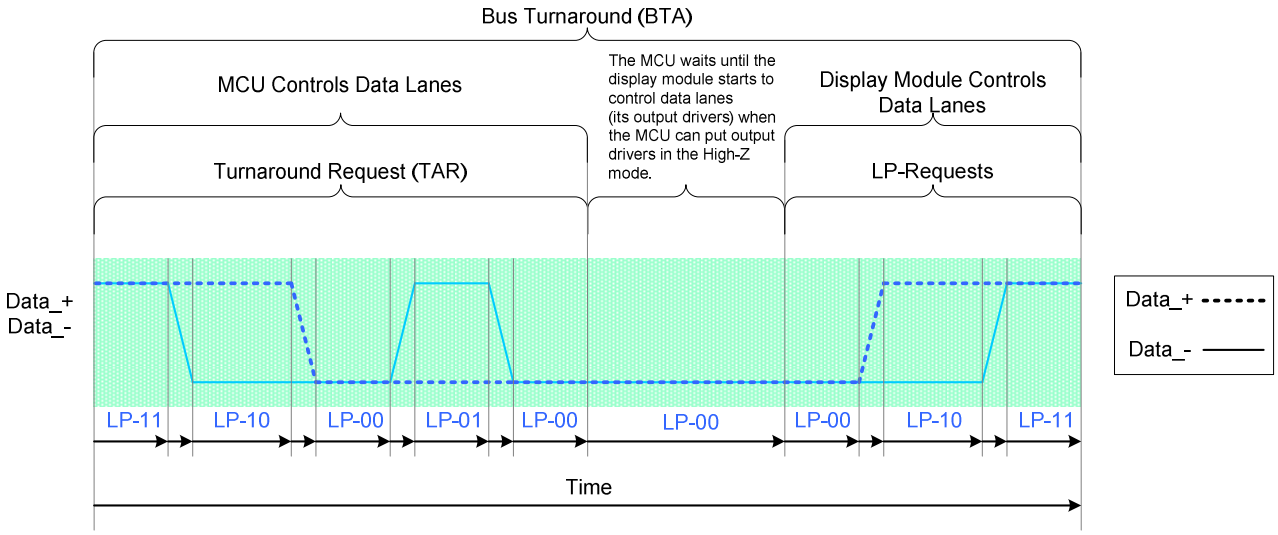
• Start (MCU):LP-11

• Turnaround Request (MCU): LP-11 _ LP-10 _ LP-00 _ LP-10 _ LP-00

• The MCU wait until the display module is starting to control DSI-D0+/- data lanes and the MCU stop to control DSI-D0+/- data lanes (=High-Z)

• The display module changes to the stop mode: LP-00 _ LP-10 _ LP-11

The same bus turnaround .procedure (From the MCU to the display module) is illustrated below.



Bus Turnaround Procedure

MCU and the display module terms are switched on above figure, if the Bus Turnaround (BTA) is from the display module to the MCU..

8.2.9. Packet Level Communication

8.2.9.1 Short Packet (SPA) And Long Packet (LPA) Structure

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

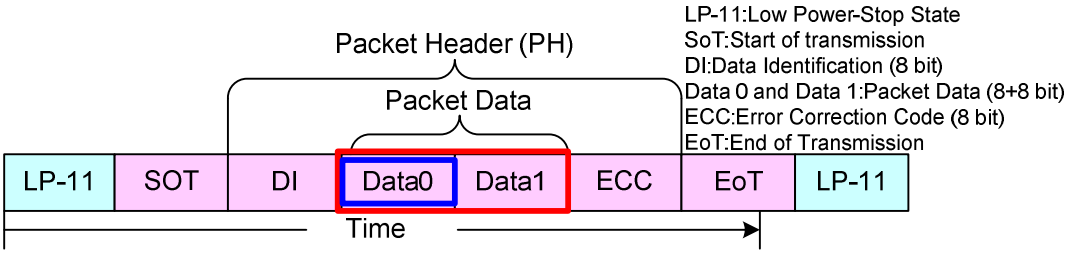
The lengths of the packets are

• Short Packet (SPa): 4 bytes

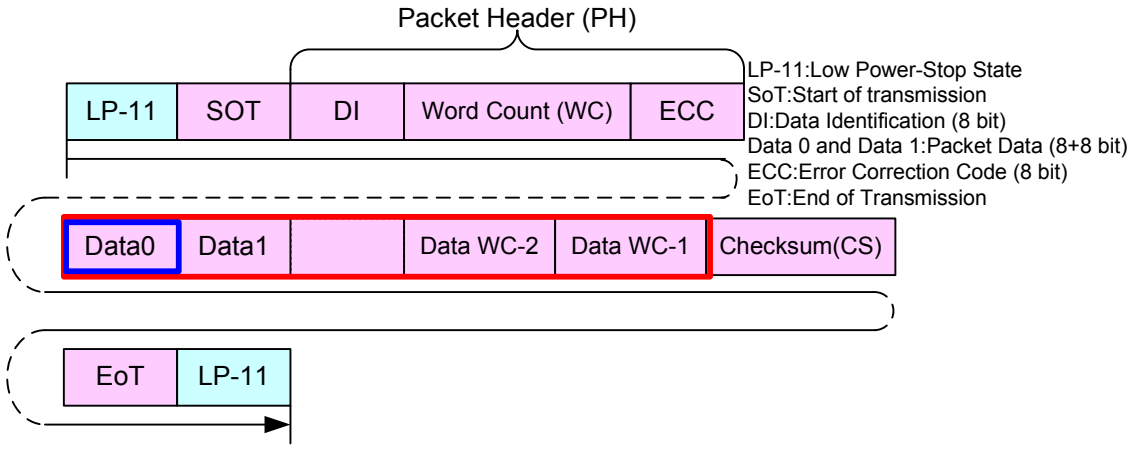
• Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

Short Packet (Spa) Structure:



Long Packet (Spa) Structure:



Note:

Short Packet (SPa) Structure and Long Packet (LPa) Structure are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sendings).

The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format e.g.

** LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11*

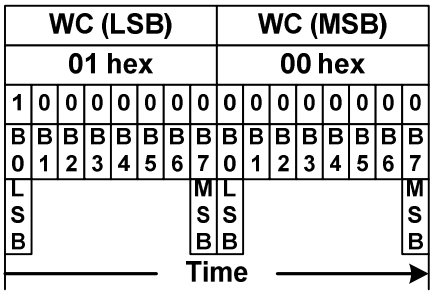
** LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11*

** LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11*

8.2.9.2 Bit Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.



Byte Order of the Multiple Byte on Packets

8.2.9.3 Pack Header (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short

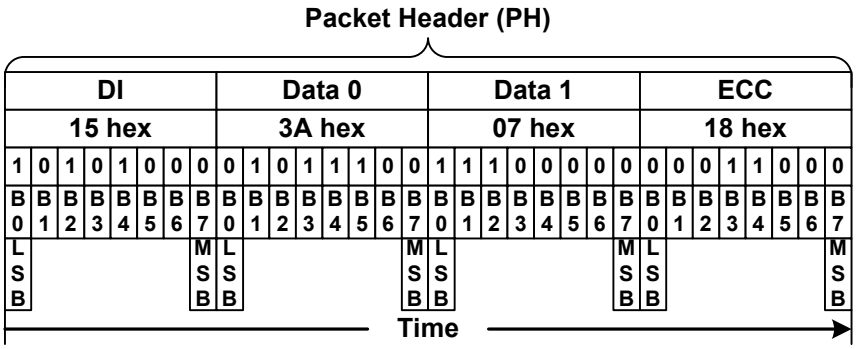
Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

• 1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)

• 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1

• 4th byte: Error Correction Code (ECC)



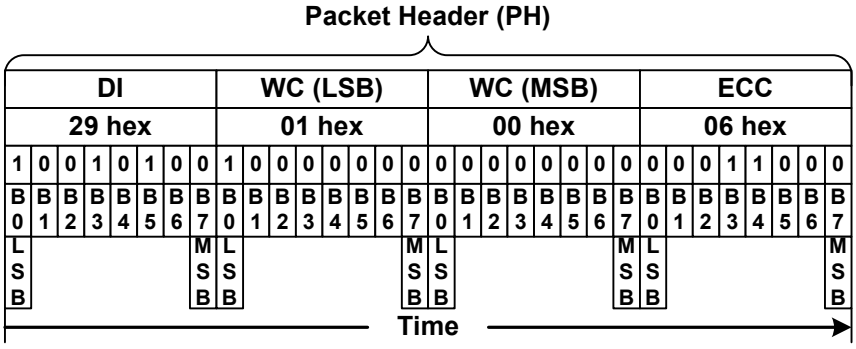
Packet Header (PH) on Short Packet(Spa)

Long Packet (LPa):

• 1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)

• 2nd and 3rd bytes: Word Count (WC)

• 4th byte: Error Correction Code (ECC)



Packet Header (PH) on Long Packet (LPa)

- Data Identification(DI)

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

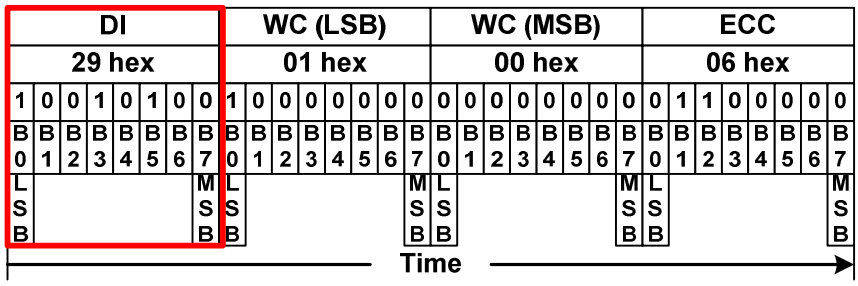
• Virtual Channel (VC), 2 bits, DI[7...6]

• Data Type (DT), 6 bits, DI[5…0]

The Data Identification (DI) structure is illustrated on a table below.

Data Identification (DI)							
Virtual Channel (VC)		Data Type (DT)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Data Identification (DI) Structure

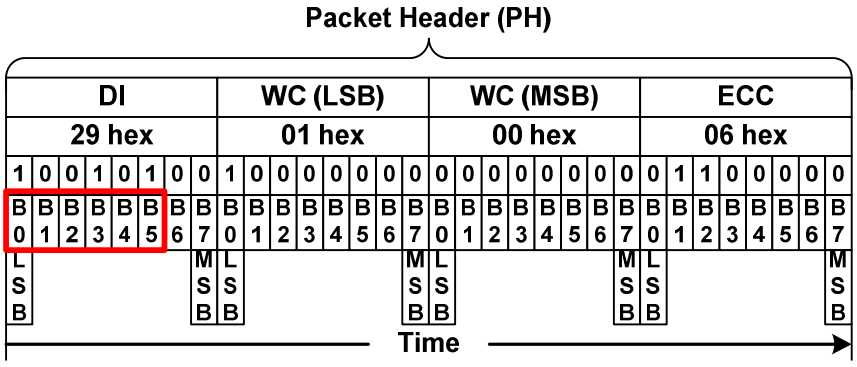


Data Identification (DI) on the Packet Header(PH)

- Data Type(DT)

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.



Data Type (DT) on the Packet Header (PH)

This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa.

These Data Type (DT) are defined on tables below.

Data Type Hex	Data Type Binary	Description	Packet Size
01h	00 0001	Sync Event, V Sync Start.	Short
11h	01 0001	Sync Event, V Sync End.	Short
21h	10 0001	Sync Event, H Sync Start.	Short
31h	11 0001	Sync Event, H Sync End.	Short
08h	00 1000	End of Transmission (EoT) packet.	Short
02h	00 0010	Color Mode (CM) Off Command.	Short
12h	01 0010	Color Mode (CM) On Command.	Short
22h	10 0010	Shut Down Peripheral Command.	Short
32h	11 0010	Turn On Peripheral Command.	Short
03h	00 0011	Generic Short WRITE, no parameters	Short
13h	01 0011	Generic Short WRITE, 1 parameter.	Short
23h	10 0011	Generic Short WRITE, 2 parameters.	Short
04h	00 0100	Generic READ, no parameters.	Short
14h	01 0100	Generic READ, 1 parameter.	Short
24h	10 0100	Generic READ, 2 parameters.	Short
05h	00 0101	DCS WRITE, no parameter.	Short
15h	01 0101	DCS WRITE, 1 parameter.	Short
06h	00 0110	DCS READ, no parameter.	Short
37h	11 0111	Set Maximum Return Packet Size.	Short
09h	00 1001	Null Packet, no data.	Long
19h	01 1001	Blanking Packet, no data.	Long
29h	10 1001	Generic Long Write.	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet.	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB,5-6-5 Format.	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB,6-6-6 Format.	Long
2Eh	10 1110	Loosely Packed Pixel Stream,18-bit RGB,6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream,24-bit RGB,8-8-8 Format.	Long

Data Type (DT) from MCU to the Display Module (or Other Devices)

From the Display Module (or Other Devices) to the MCU									
Hex	B5	B4	B3	B2	B1	B0	Description	Packet	Abbreviation
02h	0	0	0	0	1	0	Acknowledge with Error Report	Short	AwER
1Ch	0	1	1	1	0	0	DCS Read Long Response	Short	DCSRR_L
21h	1	0	0	0	0	1	DCS Read Short Response, 1 byte returned	Short	DCSRR1_S
22h	1	0	0	0	1	0	DCS Read Short Response, 2 byte returned	Short	DCSRR2_S
1Ah	0	1	1	0	1	0	Generic Read Long Response	Short	GENRR-L
11h	0	1	0	0	0	1	Generic Read Short Response,1 byte returned	Short	GENRR1-S
12h	0	1	0	0	1	0	Generic Read Short Response,2 byte returned	Short	GENRR2-S

Data Type (DT) from the Display Module (or Other Devices) to the MCU

The receiver will ignore other Data Type (DT) if they are not defined on tables: “Data Type (DT) from the MCU to the Display Module (or Other Devices)” or “ Data Type (DT) from the Display Module (or Other Devices) to the MCU”.

- Packet Data (PD) on the Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send.

The Word Count (WC) indicates the number of Bytes of Packet of Packet Data (PD) send after the Packet Header.

Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last.

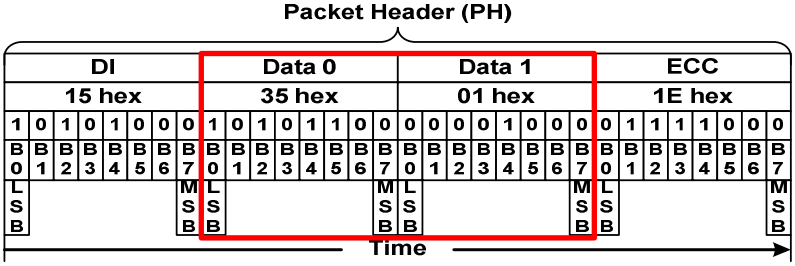
Bits of Data 1 are set to ‘0’ if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

Packet Data (PD) information:

• Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI(Data Type (DT)) = 15hex)

• Data 1: 01hex (DCS’s parameter)

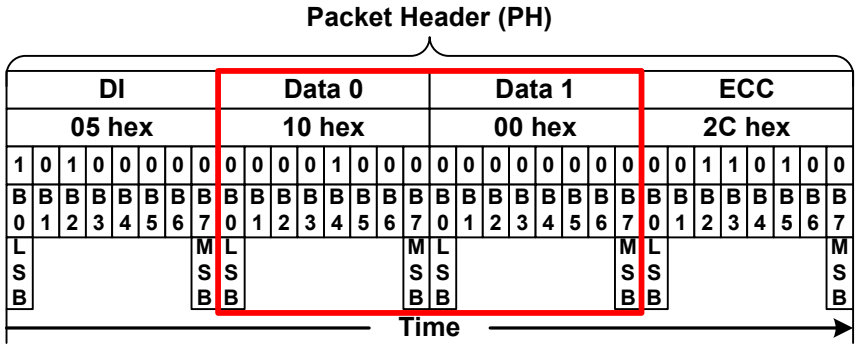


Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:

• Data 0: 10hex (DCS without parameter => DI(Data Type (DT)) = 05hex)

• Data 1: 00hex (Null)



Packet Data(PD) fo Short Packet (Spa), 1 Bytes Information

- Word Count(WC) on the Long Packet(LPa)

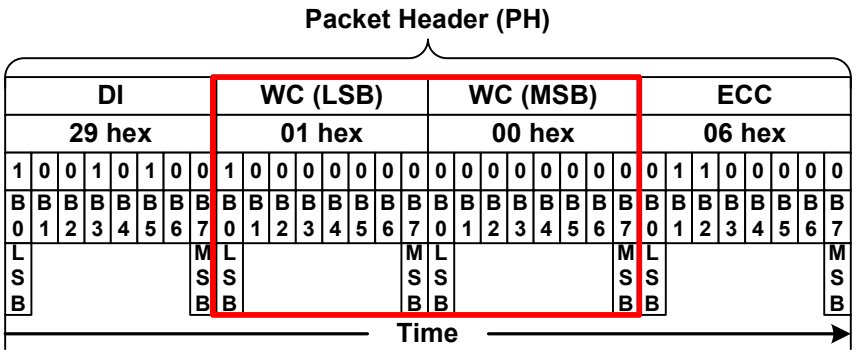
Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send.

Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH).

Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

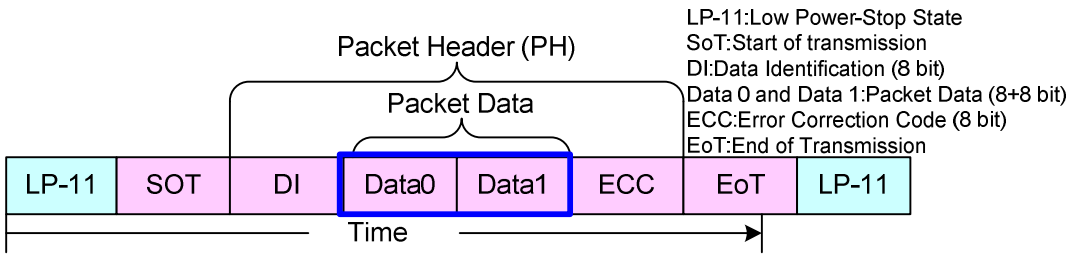
These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.

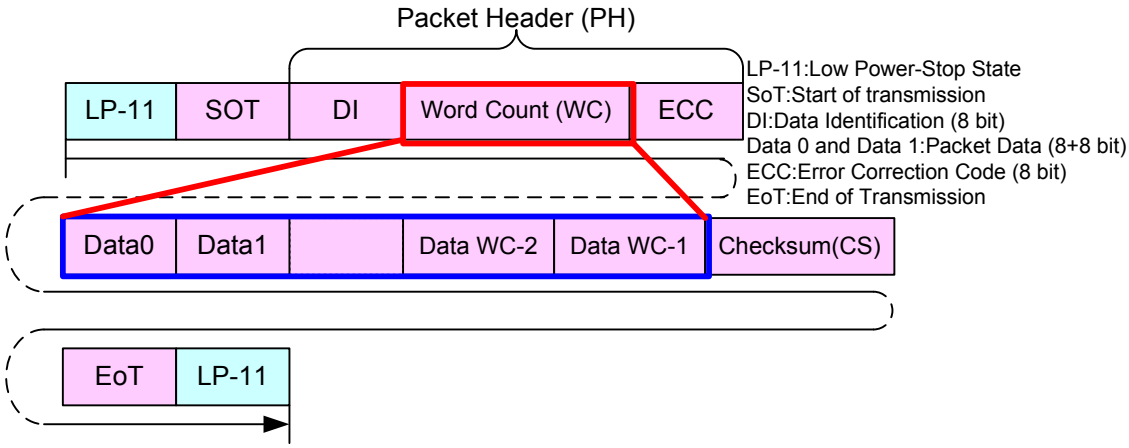


Word Count (WC) on the Long Packet (LPa)

Short Packet:



Long Packet:



- Error Correction Code (ECC)

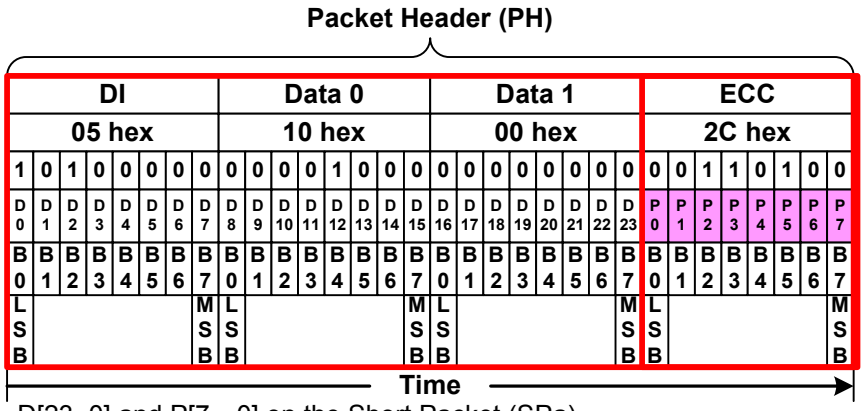
Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors on the Packet Header (PH):

The ECC protects the following field"

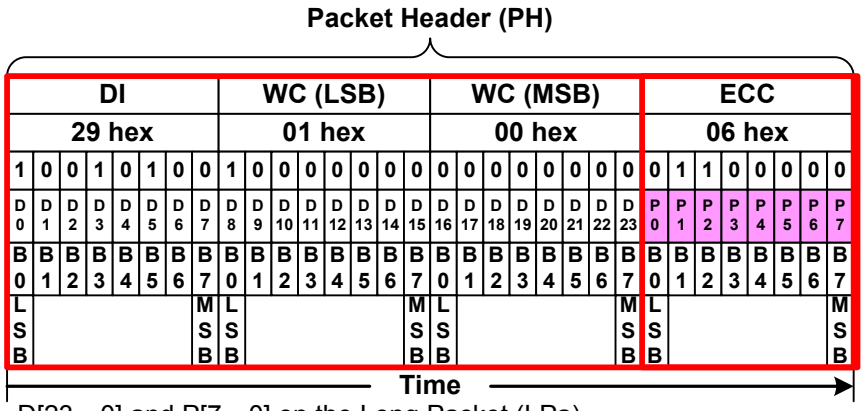
• Short Packet (SPa): Data Identification (DI) byte (8 bits, D[0...7]), Packet Data (PD) bytes (16 bits, D[8...23]) and ECC(8 bits: P[0…7])

• Long Packet (LPa): Data Identification (DI) byte (8 bits, D[0…7]), Word Count (WC) bytes (16 bits: D[8…23]) and ECC (8 bits, P[0…7])

D[23…0] and P[7…0] are illustrated for reference purposes below.



D[23..0] and P[7⋯0] on the Short Packet (SPa)



D[23⋯0] and P[7⋯0] on the Long Packet (LPa)

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function

(Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

• P7 = 0

• P6 = 0

• P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

• P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

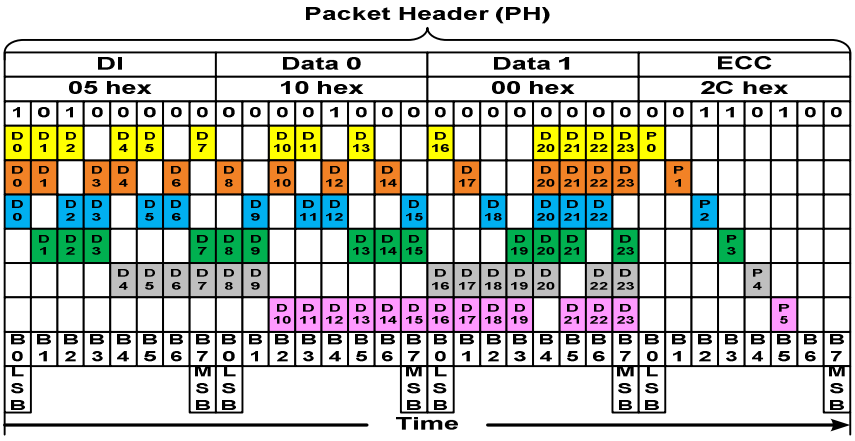
• P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

• P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

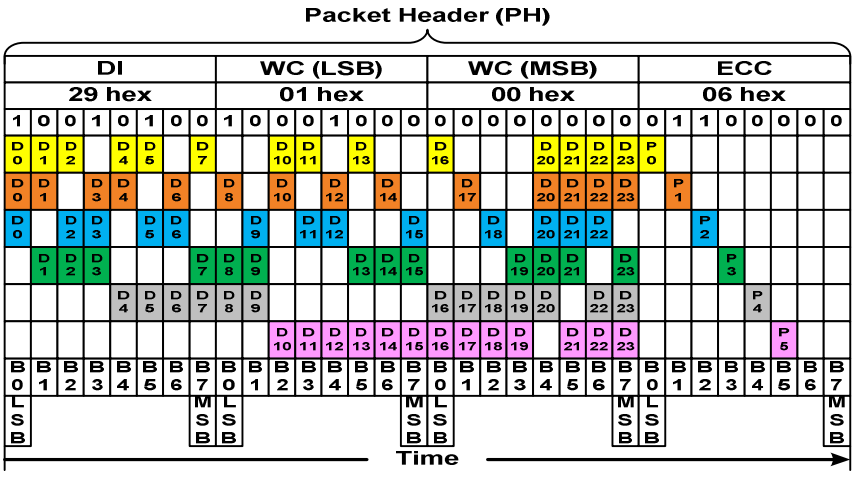
• P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

• P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D[23…0]). Therefore, there is only needed 6 bits (P[5…0]) for Error Correction Code (ECC).



XOR Functionality on the Short Packet (SPa)

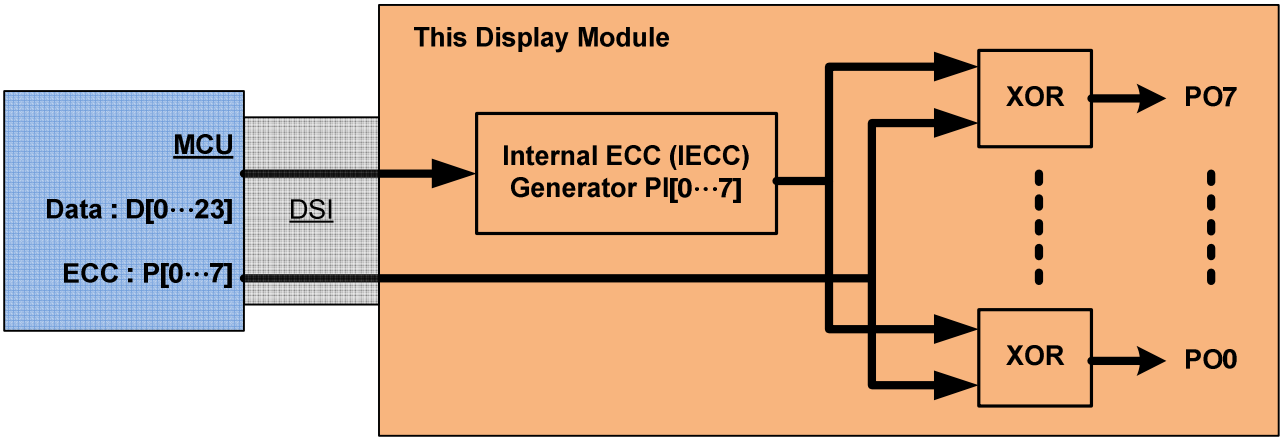


XOR Functionality on the Long Packet (LPa)

The transmitter (The MCU or the Display Module) is sending data bits D[23…0] and Error Correction Code (ECC) P[7…0]. The receiver (The Display module or the MCU) is calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7…0].

This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated for

reference purposes below.



Internal Error Correction Code (IECC) on the Display Module (The Receiver)

The sent data bits (D[23…0]) and ECC (P[7…0]) are received correctly, if a value of the PO[7…0]) is 00h. The sent data bits (D[23…0]) and ECC (P[7…0]) are not received correctly, if a value of the PO[7…0]) is not 00h.

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	0	0	0	0	0	0	03h
XOR(ECC,IECC) =>PO[7…0]	0	0	0	0	0	0	0	0	=00h=>No Error
	L S B							M S B	

Internal XOR Calculation between ECC and IECC Values-No Error

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC,IECC) =>PO[7…0]	0	0	1	1	0	0	0	0	=0Ch=> Error
	L							M	
	S							S	
	B							B	

Internal XOR Calculation between ECC and IECC Values- Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[23…0] on the transmitter side.

The number of the errors (one or more) can be defined when the value of the PO[7…0] is compared to values on the following table.

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

One error is detected if the value of the PO[7…0] is on : One Bit Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

• PO[7…0] = 0Eh

• The bit of the data (D[23…0]), what is not correct, is D[3]

More than one error is detected if the value of the PO[7…0] is not on: One Bit Error Value of the Error Correction Code (ECC) e.g. PO[7…0] =

8.2.9.4 Packet Data (PD) on the Long Packet (LPa)

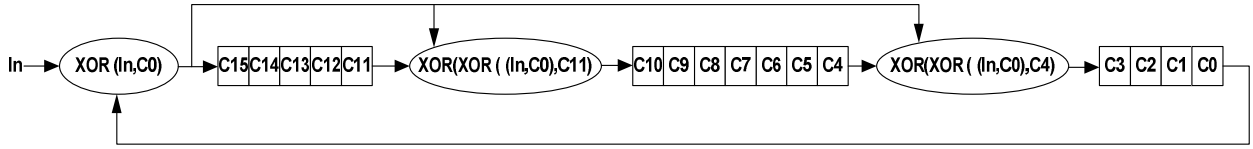
Packet Data (PD) of the Long Packet (LPa) is defined after Packet Header (PH) of the Long Packet (LPa). The number of the data bytes is defined on chapter “Word Count (WC) on the Long Packet (LPa)”.

8.2.9.5 Packet Footer (PF) on the Long Packet (LPa)

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa).

The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial

X16+X12+X5+X0 as it is illustrated below.

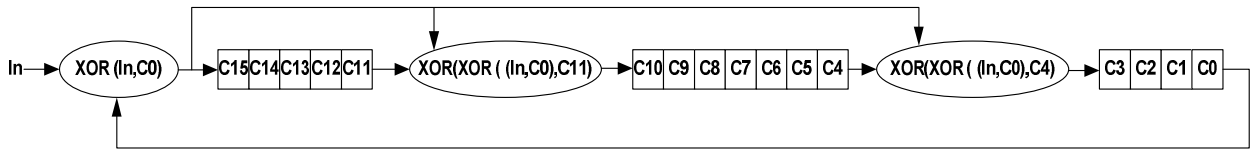


16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Least Significant Bit (LSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is

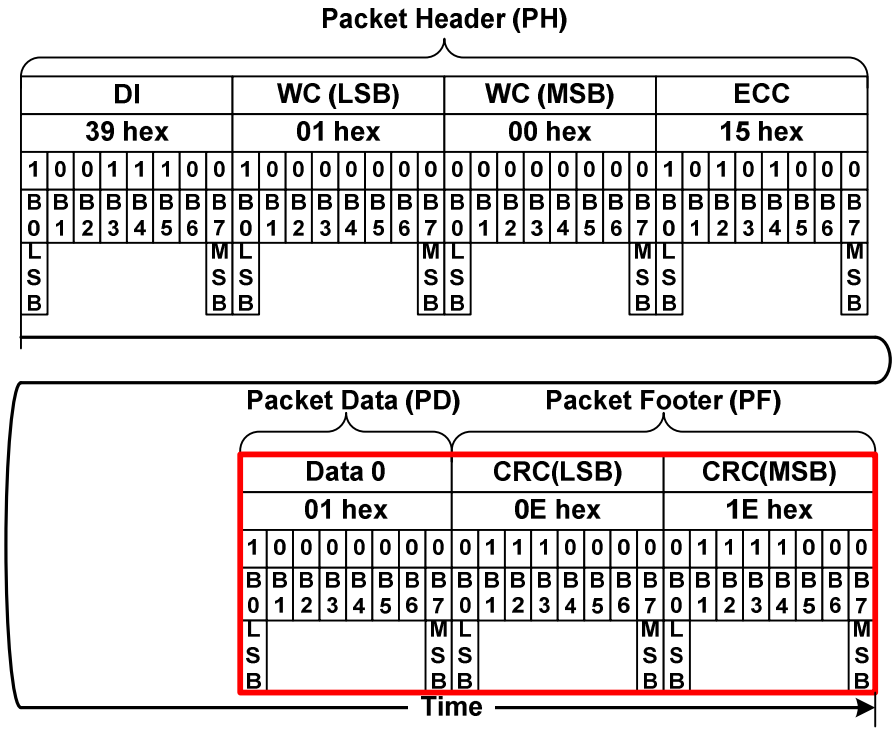
01h, is illustrated (step-by-step) below.



Stop	In	XOR(In,C0)	C15	C14	C13	C12	C11	XOR(XOR(In,C0),C11(Step-1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In,C0),C4(Step-1))	C3	C2	C1	C0	C0
0	X	X	1	1	1	1	1	X	1	1	1	1	1	1	1	X	1	1	1	1	X
1	1(LSB)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
5	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
6	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
7	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0
8	0(MSB)	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
	1 Byte	CRC Resoult	0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0	
			LSB																	LSB	

CRC Calculation – Packet Data (PD) is 01h

A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.



Packet Footer (PF) Example

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

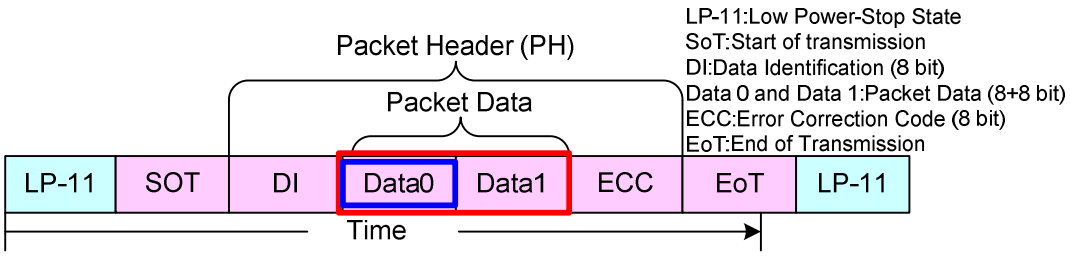
8.3. Packet Transmission

8.3.1 Packet from the MCU to the Display Module

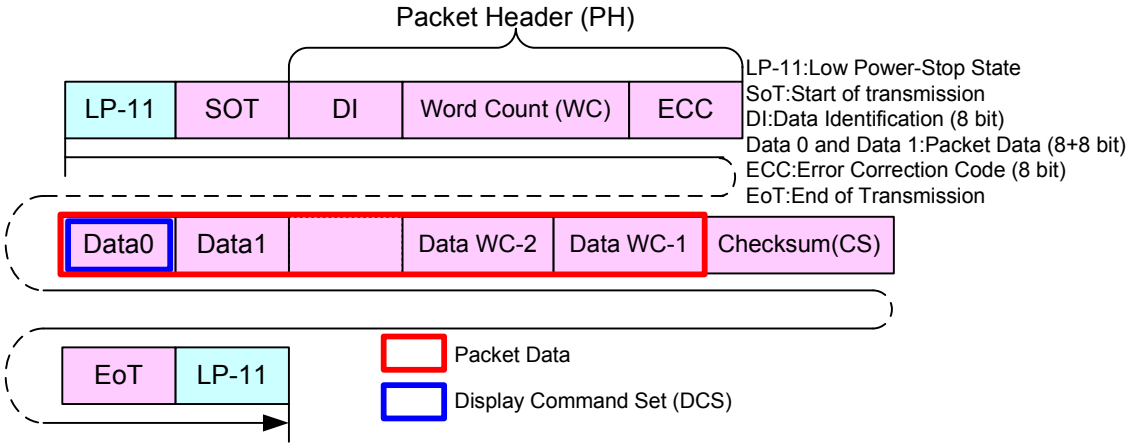
- Display Command Set (DCS)

Display Command Set (DCS), which is defined on chapter “9 Instruction Description”, is used from the MCU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD),which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated below.

Short Packet:



Long Packet:



Display Command Set (DCS) on Short Packet (SPa) and Long Packet (LPa)

- Generic Write, 1 Parameter (GENW1-S), Data Type = 01 0011 (13h)

"Generic Write, 1 Parameter" (GENW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0011b), from the MCU to the display module. The content of 2 payload bytes is "command" and 00h.

These commands are defined on a table (See chapter "9 Instruction Description") below

Command
NOP (00h)
SWRESET (01h)
SLPIN (10H)
SLPOUT (11h)
PTLON (12h)
NORON (13h)
INVOFF (20h)
INVON (21h)
ALLPOFF (22h)
ALLPON (23h)
DISPOFF (28h)
DISPON (29h)
IDMOFF (38h)
IDMON (39h)

Short Packet (SPa) is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 01 0011b

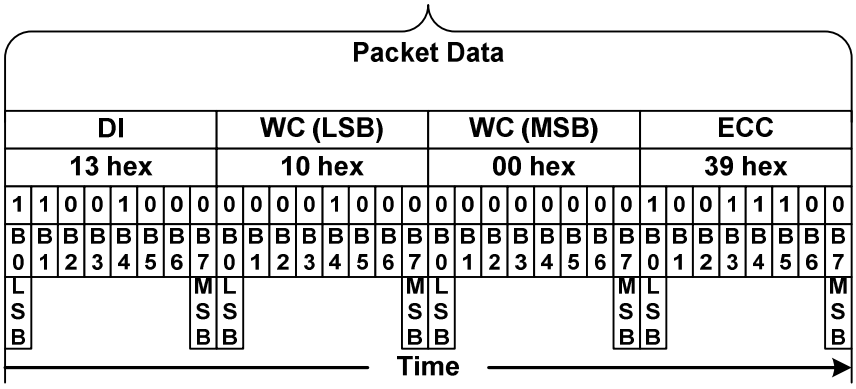
• Packet Data (PD)

  • Data 0: "Sleep In (10h)", Display Command Set (DCS)

  • Data 1: Always 00hex

• Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Generic Write,1 Parameter (GENW1-S)-Example

- Generic Write, 2 Parameter (GENW2-S), Data Type = 10 0011 (23h)

"Generic Write, 2 Parameter" (GENW2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0011b), from the MCU to the display module. The content of 2 payload bytes is "command" and "parameter". These commands are defined on a table (See chapter "6 Instruction Description") below.

Command
GAMSET (26h)
COLMOD (3Ah)
WRDISBV (51h)
WRCTRLD (53h)
WRCABC (55h)
WRCABCMB (5Eh)

Short Packet (SPa) is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 10 0011b

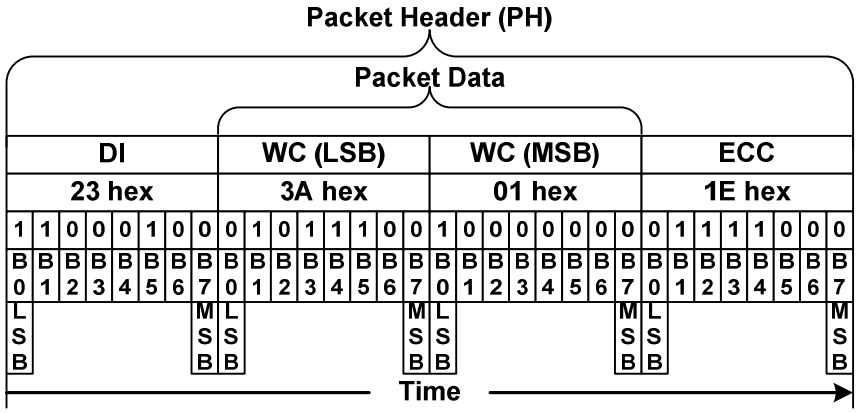
• Packet Data (PD)

  • Data 0: "PMCSET (3Ah)", Display Command Set (DCS)

  • Data 1: 01hex, Parameter of the DCS

• Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Generic Write, 2 Parameter (GENW2-S) – Example

- Generic Write Long (GENW-L) , Data Type = 10 1001 (29h)

"Generic Write Long" (GENW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 10 1001b), from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters), are defined on a table (See chapter "6 Instruction Description") below.

Command		
NOP (00h) , Note1	INVON (21h) , Note1	IDMOFF (38h) , Note1
SWRESET (01h) , Note1	ALLPOFF (22h)	IDMON (39h) , Note1
SLPIN (10H) , Note1	ALLPON (23h)	COLMOD (3Ah) , Note2
SLPOUT (11h) , Note1	GAMSET (26h), , Note2	WRDISBV (51h) , Note2
PTLON (12h) , Note1	DISPOFF (28h) , Note1	WRCTRLD (53h) , Note2
NORON (13h) , Note1	DISPON (29h) , Note1	WRCABC (55h) , Note2
INVOFF (20h) , Note1	PARLINES (C5h)	WRCABCMB (5E) , Note2

Notes : 1. Also Short Packet (SPa) can be used; See Generic Write, 1 Parameter.

2. Also Short Packet (SPa) can be used; See Generic Write, 2 Parameter.c

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 10 1001b

• Word Count (WC)

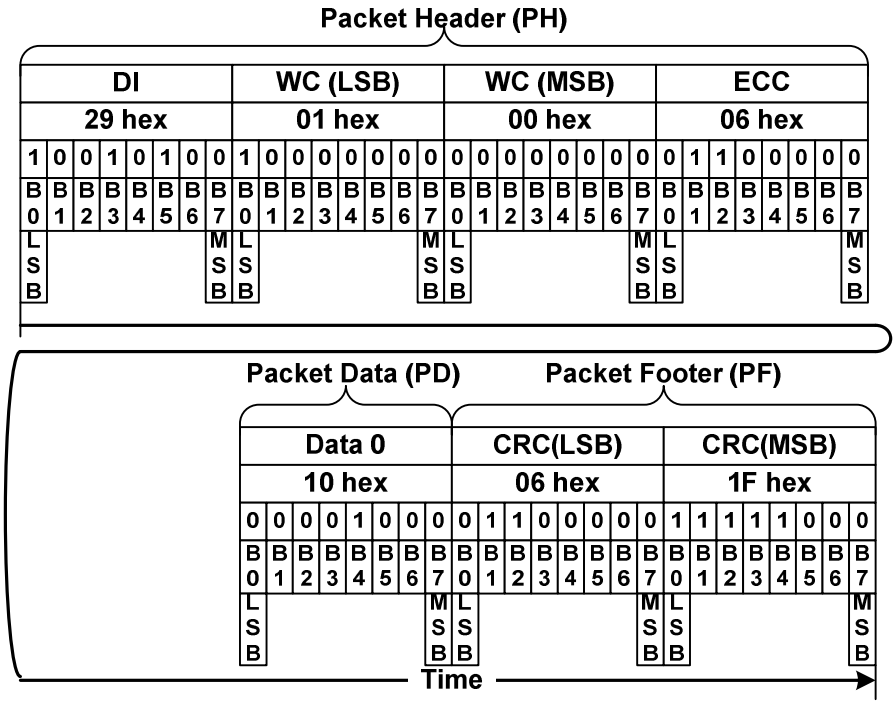
  • Word Count (WC): 0001h

• Error Correction Code (ECC)

• Packet Data (PD): Data 0: "Sleep In (10h)", Display Command Set (DCS)

• Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.



Generic Long Write(GENW-L) with DCS Only – Example

Long Packet (LPa), when a Write (1 parameter) was sent, is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 10 1001b

• Word Count (WC)

  • Word Count (WC): 0002h

• Error Correction Code (ECC)

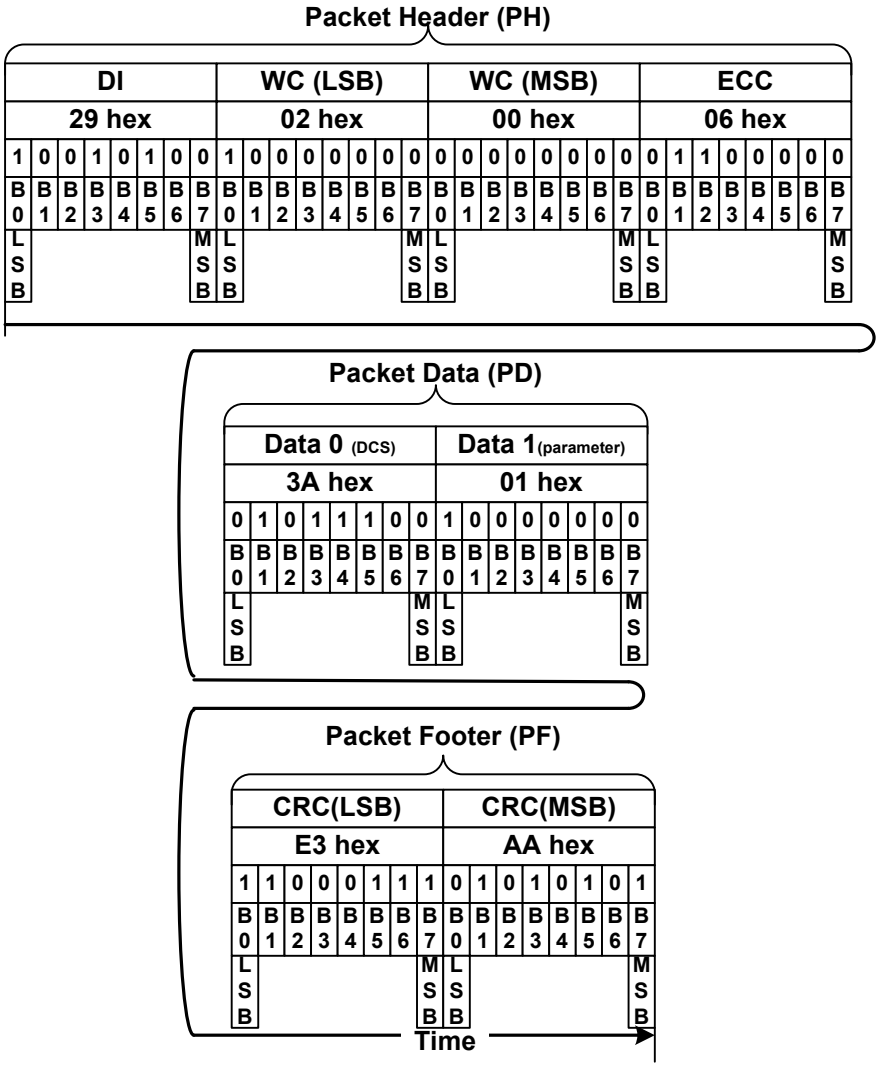
• Packet Data (PD):

  • Data 0: “Gamma Set (3Ah)”, Display Command Set (DCS)

  • Data 1: 01hex, Parameter of the DCS

• Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.



Generic Long Write (GENW-L) with DCS and 1 Parameter-Example

Long Packet (Lpa), when a Write (4 parameters) was sent, is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 10 1001b

• Word Count (WC)

  • Word Count (WC): 0005h

• Error Correction Code (ECC)

• Packet Data (PD):

  • Data 0: “PARLINES (30h)”, Display Command Set (DCS)

  • Data 1: 00hex, 1st Parameter of the DCS, Start Column SC[15…8]

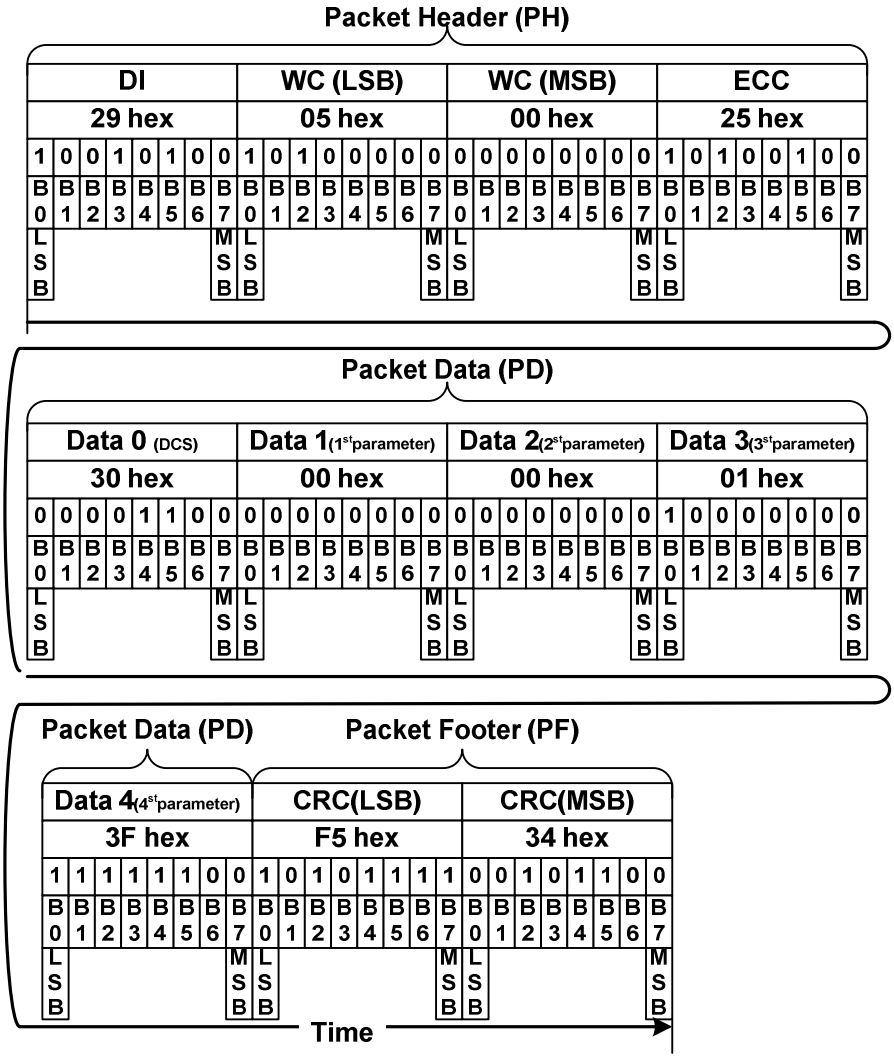
  • Data 2: 00hex, 2nd Parameter of the DCS, Start Column SC[7…0]

  • Data 3: 01hex, 3rd Parameter of the DCS, End Column EC[15…8]

  • Data 4: 3Fhex, 4th Parameter of the DCS, End Column EC[7…0]

• Packet Footer (PF)

This is defined on the Long Packet (Lpa) as follows.



Generic Write Long (GENW-L) with DCS and 4 Parameters-Example

- Generic Read , 1 Parameter (GENR1-S) , Data Type = 01 0100 (14h)

"Generic Read, 1 Parameter (GENR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT,01 0100b), from the MCU to the display module. This command is defined on a table (See chapter "9 Instruction Description") below.

Command	
RDDID (04h)	RDDSM (0Eh)
RDNUMED (05h)	RDDSDR (0Fh)
RDRED (06h)	RDDISBV (52h)
RDGREEN (07h)	RDCTRLD (54h)
RDBLUE (08h)	RDCABC (56h)
RDDPM (0Ah)	RDCABCMB (5Fh)
RDDMADCTR (0Bh)	RDID1 (DAh)
RDDCOLMOD (0Ch)	RDID2 (DBh)
RDDIM (0Dh)	RDID3 (DCh)

The MCU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send "Display Command Set (DCS) Read, No Parameter" to the display module. This same sequence is illustrated for reference purposes below.

Step 1:

• The MCU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

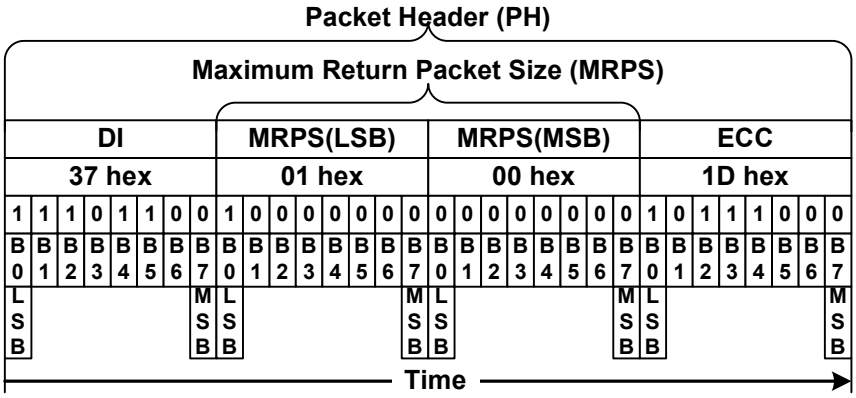
  • Data Type (DT, DI[5…0]): 11 0111b

• Maximum Return Packet Size (MRPS)

  • Data 0: 01hex

  • Data 1: 00hex

• Error Correction Code (ECC)



Set Maximum Return Packet Size (SMRPS-S)- Example

Step 2:

• The MCU wants to receive a value of the “Read ID1 (DAh)” from the display module when the MCU sends “Generic Read, 1 Parameter” to the display module

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

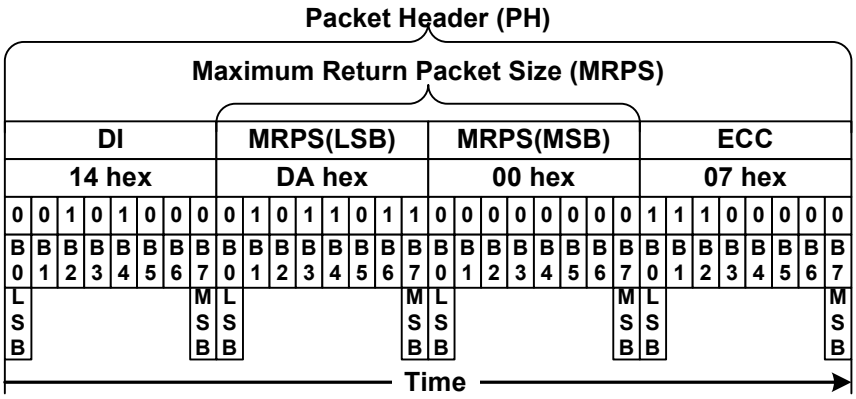
  • Data Type (DT, DI[5…0]): 01 0100b

• Packet Data (PD)

  • Data 0: “Read ID1 (DAh)”, Display Command Set (DCS)

  • Data 1: Always 00hex

• Error Correction Code (ECC)



Generic Read, 1 Parameter (GENR1-S) – Example

Step 3: The display module can send 2 different information to the MCU after Bus Turnaround (BTA)

1. An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command. See section “Acknowledge with Error Report (AwER)”.

2. Information of the received command. Short Packet (SPa) or Long Packet (LPa)

- Display Command Set (DCS) Write, No Parameter (DCSWN-S) , Data Type = 00 0101 (05h)

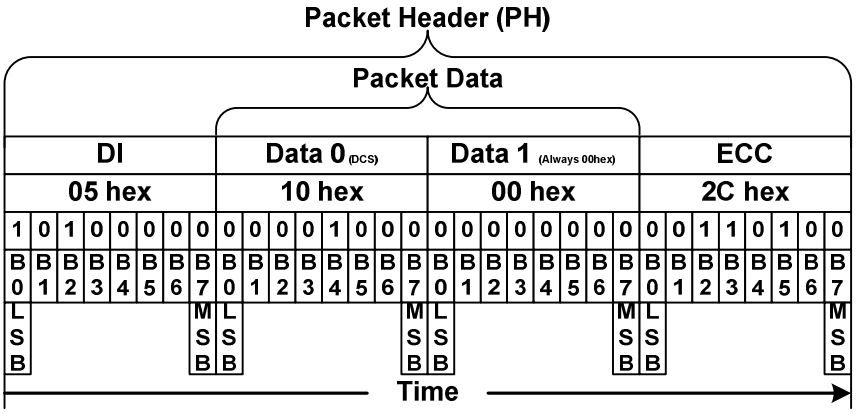
“Display Command Set (DCS) Write, No Parameter” is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0101b), from the MCU to the display module. These commands are defined on a table (See chapter “9 Instruction Description”) below.

Command	
NOP (00h)	INVON (21h)
SWRESET (01h)	ALLPOFF (22h)
SLPIN (10h)	ALLPON (23h)
SLPOUT (11h)	DISPOFF (28h)
PTLON (12h)	DISPON (29h)
NORON (13h)	IDMOFF (38h)
INVOFF (20h)	IDMON (39h)

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 00 0101b
- Packet Data (PD)
  - Data 0: “Sleep In (10h)”, Display Command Set (DCS)
  - Data 1: Always 00hex
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Display Command Set (DCS) Write,No Parameter(DCSWN-S)-Example

- Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) , Data Type = 01 0101 (15h)

"Display Command Set (DCS) Write, 1 Parameter" (DCSW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0101b), from the MCU to the display module. These commands are defined on a table (See chapter "9 Instruction Description") below.

Command
GAMSET (26h)
COLMOD (3Ah)
WRDISBV (51h)
WRCTRLD (53h)
WRCABC (55h)
WRCABCMB (5Eh)

Short Packet (SPa) is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 01 0101b

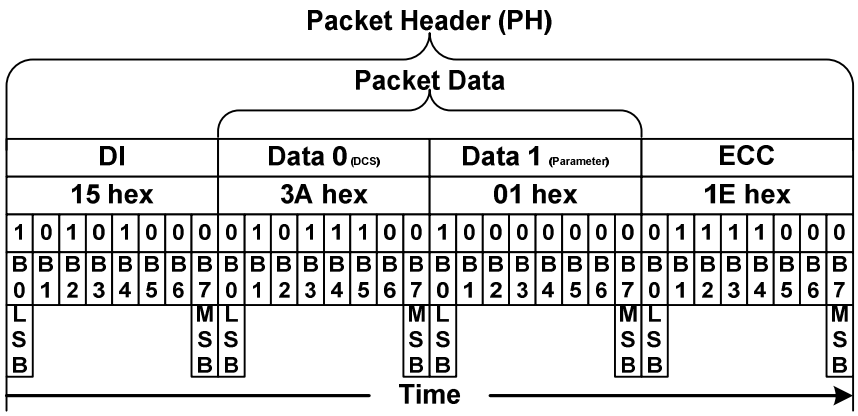
• Packet Data (PD)

  • Data 0: "PMCSET (3Ah)", Display Command Set (DCS)

  • Data 1: 01hex, Parameter of the DCS

• Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Display Command Set (DCS) Write,1 Parameter (DCSW1-S)-Example

- Display Command Set (DCS) Write Long (DCSW-L) , Data Type = 11 1001 (39h)

"Display Command Set (DCS) Write Long" (DCSW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 11 1001b), from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters), are defined on a table (See chapter "9 Instruction Description") below

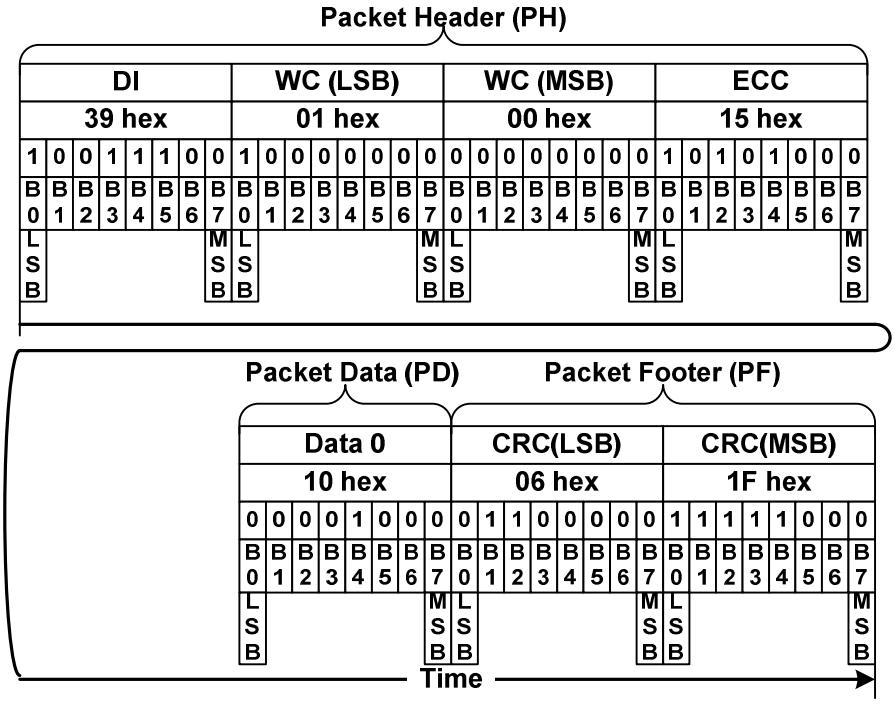
Command		
NOP (00h) , Note1	INVON (21h) , Note1	COLMOD (3Ah) , Note2
SWRESET (01h) , Note1	GAMSET (26h) , Note2	WRDISBV (51h), Note2
SLPIN (10h) , Note1	DISPOFF (28h) , Note1	WRCTRLD (53h)
SLPOUT (11h) , Note1	DISPON (29h), Note1	WRCABC (55h) , Note2
PTLON (12h) , Note1	PARLINES (30h)	WRCABCMB (5Eh)
NORON (13h), Note1	IDMOFF (38h) , Note1	-
INVOFF (20h), Note1	IDMON (39h) , Note1	-

Notes：1. Also Short Packet (SPa) can be used; See_Display Command Set (DCS) Write, No Parameter.
2. Also Short Packet (SPa) can be used; See Display Command Set (DCS) Write, 1 Parameter.

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

• Data Identification (DI)
  • Virtual Channel (VC, DI[7…6]): 00b
  • Data Type (DT, DI[5…0]): 11 1001b
• Word Count (WC)
  • Word Count (WC): 0001h
• Error Correction Code (ECC)
• Packet Data (PD): Data 0: "Sleep In (10h)", Display Command Set (DCS)
• Packet Footer (PF)

This is defined on the Short Packet (SPa) as follows.



Display Command Set (DCS) Write Long (DCSW-L) with DCS Only-Example

Long Packet (LPa), when a Write (1 parameter) was sent, is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 11 1001b

• Word Count (WC)

  • Word Count (WC): 0002h

• Error Correction Code (ECC)

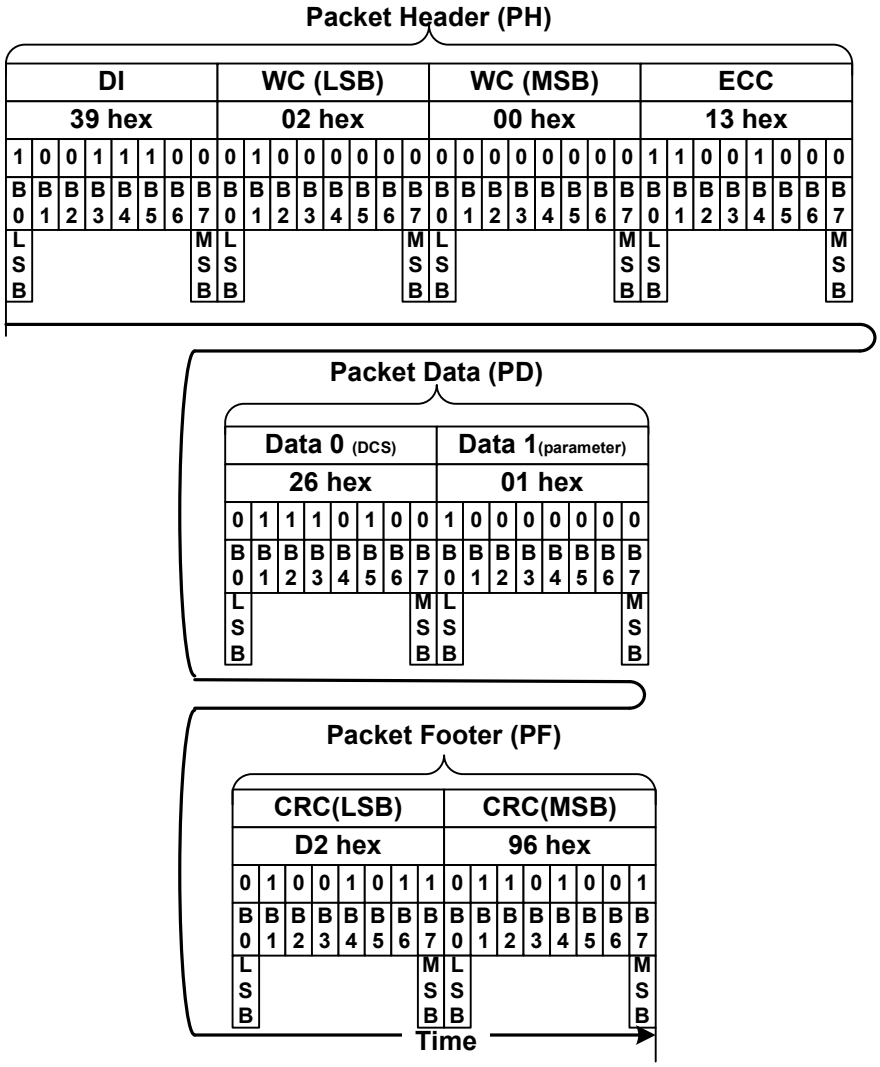
• Packet Data (PD):

  • Data 0: “Gamma Set (26h)”, Display Command Set (DCS)

  • Data 1: 01hex, Parameter of the DCS

• Packet Footer (PF)

This is defined on the Short Packet (SPa) as follows



Display Command Set (DCS) Write Long with DCS and 1 Parameter-Example

Long Packet (LPa), when a Write (4 parameters) was sent, is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 11 1001b

• Word Count (WC)

  • Word Count (WC): 0005h

• Error Correction Code (ECC)

• Packet Data (PD):

  • Data 0: “PARLINES (30h)”, Display Command Set (DCS)

  • Data 1: 00hex, 1st Parameter of the DCS, Start Column SC[15…8]

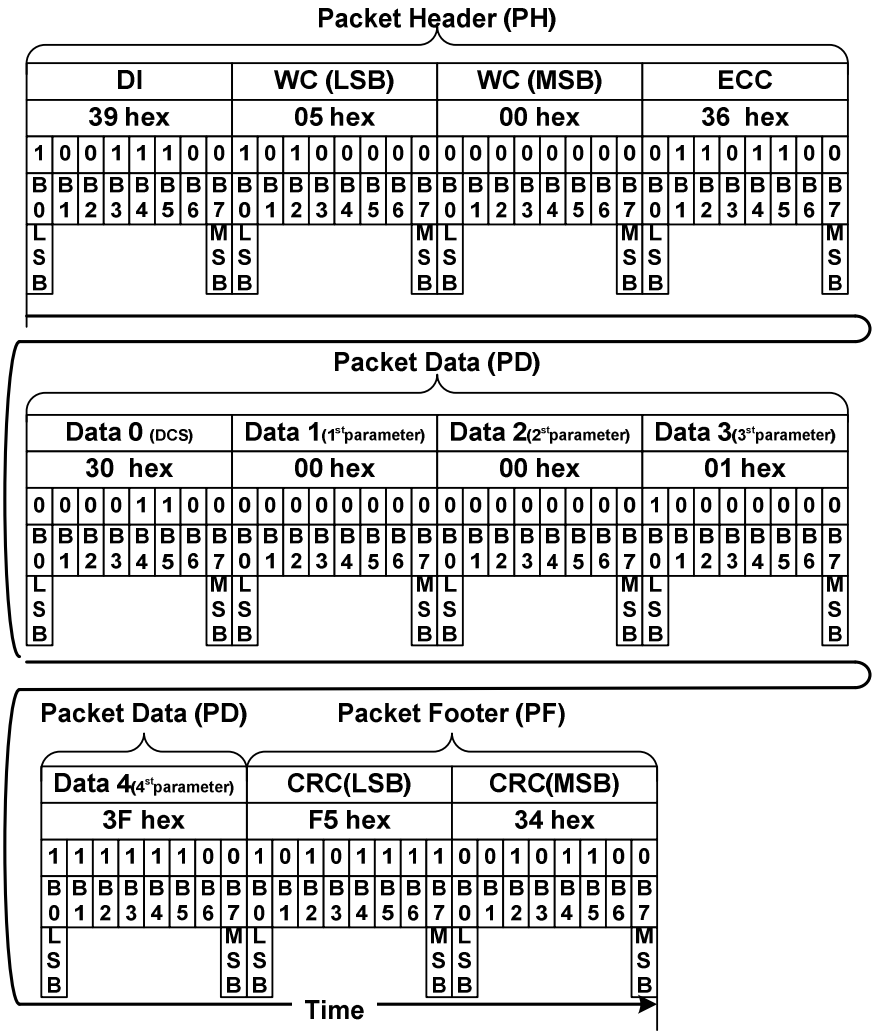
  • Data 2: 00hex, 2nd Parameter of the DCS, Start Column SC[7…0]

  • Data 3: 01hex, 3rd Parameter of the DCS, End Column EC[15…8]

  • Data 4: 3Fhex, 4th Parameter of the DCS, End Column EC[7…0]

• Packet Footer (PF)

This is defined on the Short Packet (SPa) as follows.



Display Command Set (DCS) Write Long with DCS and 4 Parameters-Example

- Display Command Set (DCS) Read, No Parameter (DCSRN-S), Data Type = 00 0110 (06h)

"Display Command Set (DCS) Read, No Parameter" (DCSRN-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0110b), from the MCU to the display module. These commands are defined on a table (See chapter "9 Instruction Description") below.

Command	
RDDID (04h)	RDDSM (0Eh)
RDNUMED (05h)	RDDSDR (0Fh)
RDRED (06h)	RDDISBV (52h)
RDGREEN (07h)	RDCTRLD (54h)
RDBLUE (08h)	RDCABC (56h)
RDDPM (0Ah)	RDCABCMB (5Fh)
RDDMADCTR (0Bh)	RDID1 (DAh)
RDDCOLMOD (0Ch)	RDID2 (DBh)
RDDIM (0Dh)	RDID3 (DCh)

The MCU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send "Display Command Set (DCS) Read, No Parameter" to the display module. This same sequence is illustrated for reference purposes below.

Step 1:

• The MCU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

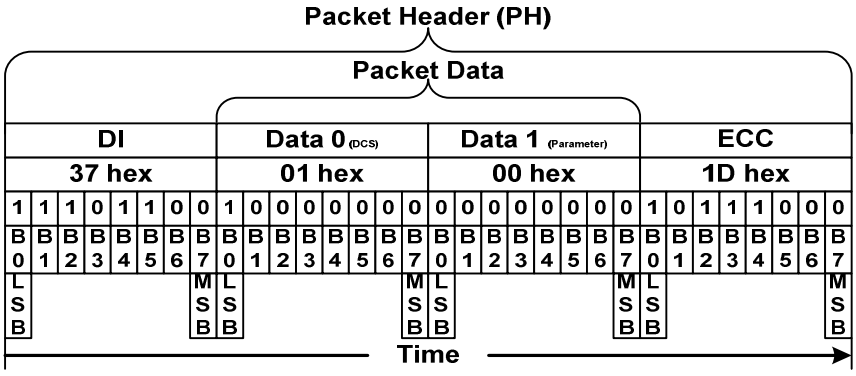
  • Data Type (DT, DI[5…0]): 11 0111b

• Maximum Return Packet Size (MRPS)

  • Data 0: 01hex

  • Data 1: 00hex

• Error Correction Code (ECC)



Set Maximum Return Packet Size (SMRPS-S) - Example

Step 2:

• The MCU wants to receive a value of the “Read ID1 (DAh)” from the display module when the MCU sends “Display Command Set (DCS) Read, No Parameter” to the display module

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

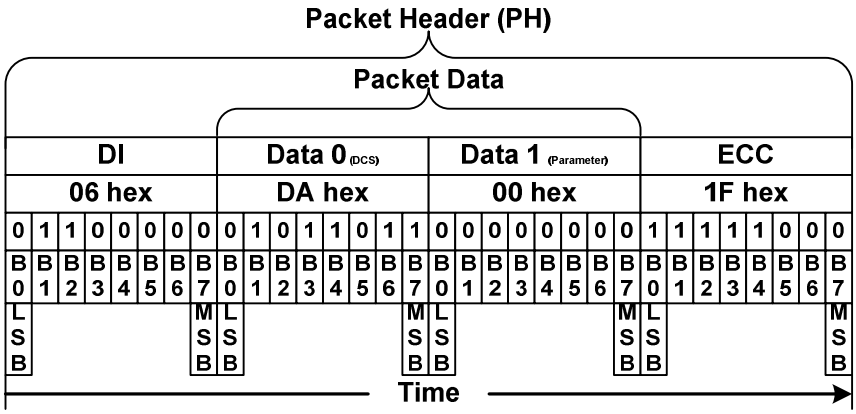
  • Data Type (DT, DI[5…0]): 00 0110b

• Packet Data (PD)

  • Data 0: “Read ID1 (DAh)”, Display Command Set (DCS)

  • Data 1: Always 00hex

• Error Correction Code (ECC)



Display Command Set (DCS) Read, No Parameter (DCSRN-S) – Example

Step 3: The display module can send 2 different information to the MCU after Bus Turnaround (BTA)

1. An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command. See section “Acknowledge with Error Report (AwER)”.

2. Information of the received command. Short Packet (SPa) or Long Packet (LPa)

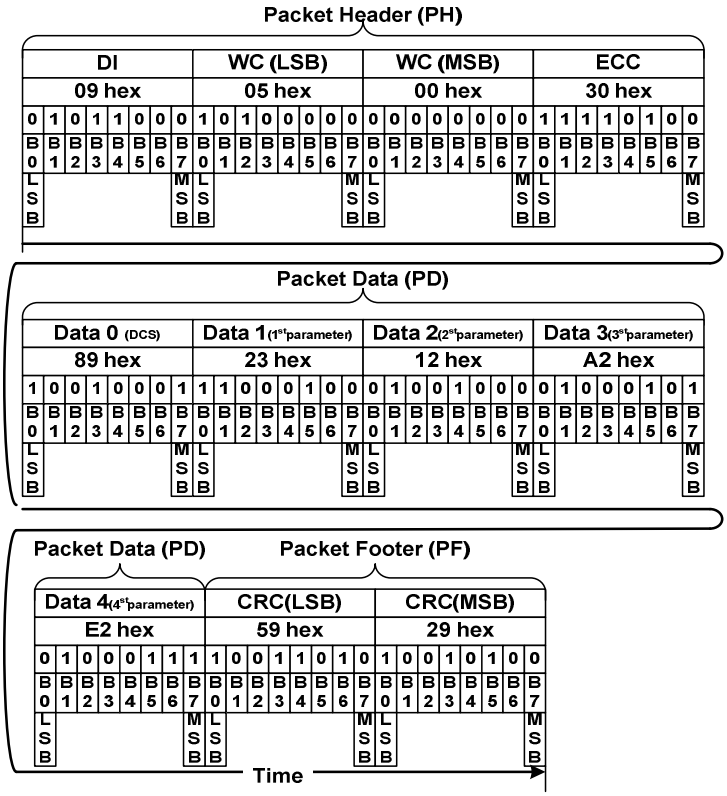
- Null Packet, No Data (NP-L) , Data Type = 00 1001 (09h)

"Null Packet, No Data" (NP-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 001001b),from the MCU to the display module. The purpose of this command is keeping data lanes in the high speed mode (HSDT), if it is needed. The display module is ignored Packet Data (PD) what the MCU is sending.

Long Packet (LPa), when 5 random data bytes of the Packet Data (PD) were sent, is defined e.g.

• Data Identification (DI)
  • Virtual Channel (VC, DI[7…6]): 00b
  • Data Type (DT, DI[5…0]): 00 1001b
• Word Count (WC)
  • Word Count (WC): 0005h
• Error Correction Code (ECC)
• Packet Data (PD):
  • Data 0: 89h (Random data)
  • Data 1: 23h (Random data)
  • Data 2: 12h (Random data)
  • Data 3: A2h (Random data)
  • Data 4: E2h (Random data)
• Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.



Null Packet, No Data (NP-L)-Example

- End of Transmission Packet (EoTP), Data Type = 00 1000 (08h)

"End of Transmission Packet" (EoTP) is always using a Short Packet (SPa), what is defined on Data Type (DT, 001000b), from the MCU to the display module. The purpose of this command is terminated the high speed mode (HPDT) properly when there is added this extra packet after the last payload packet before "End of Transmission" (EoT), which is an interface level functionality.

The MCU can decide if it want to use the "End of Transmission Packet" (EoTP) or not. The ST7701S has the capability to support both: i.e. If MCU applies the EoTP, it shall report the "DSI Protocol Violation" error when the EoTP is not detected in the high speed (HS). This error reporting can be enable/disable by bit DIS_EoTP_HS of command B100h (page 0).

The display module is or isn't receiving "End of Transmission Packet" (EoTP) from the MCU during the Low Power Data Transmission (LPDT) mode before "Marked-1" (=leaving Escape mode) what ends the Low Power Data Transmission (LPDT) mode.

The display module is not allowed to send "End of Transmission Packet" (EoTP) to MCU during the Low Power Data Transmission (LPDT) mode.

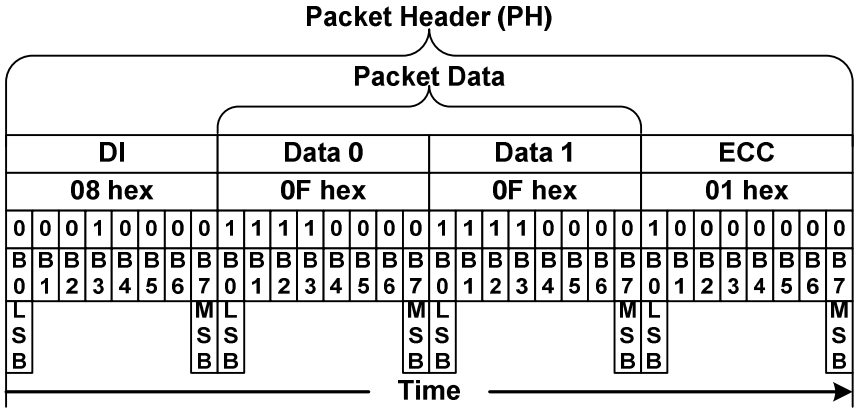
The summary of the receiving and transmitting EoTP is listed below.

Direction	Display Module (DM) in High Speed Data Transmission (HPDT)	Display Module (DM) in Low Power Data Transmission (LPDT)
MCU=>Display Driver	With or Without EoTP is Supported	With or Without EoTP is Supported
Display Driver=>MCU	HS Mode is not available (EoTP is not available)	EoTP can not be sent by the Display Driver

Receiving and Transmitting EoTP during LPDT

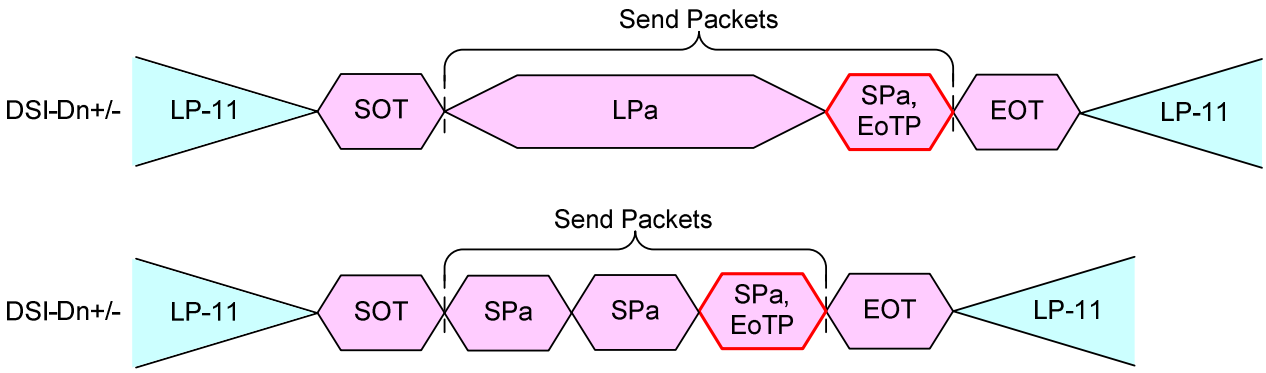
Short Packet (SPa) is using a fixed format as follow

• Data Identification (DI)
  • Virtual Channel (VC, DI[7…6]): 00b
  • Data Type (DT, DI[5…0]): 00 1000b
• Packet Data (PD):
  • Data 0: 0Fh
  • Data 1: 0Fh
• Error Correction Code (ECC)
• ECC: 01h



End of Transmission Packet (EoTP)

Some use case of the “End of Transmission Packet” (EoTP) are illustrated only for reference purpose below.



End of Transmission Packet (EoTP)-Example

- Sync Event (H Start, H End, V Start, V End), Data Type = xx 0001 (x1h)

Sync Events are Short packets and, therefore, can time-accurately represent events like the start and end of sync pulses. As “start” and “end” are separate and distinct events, the length of sync pulses, as well as position relative to active pixel data, e.g. front and back porch display timing, may be accurately conveyed to the peripheral. The Sync Events are defined as follows:

• Data Type = 00 0001 (01h) V Sync Start • Data Type = 01 0001 (11h) V Sync End

• Data Type = 10 0001 (21h) H Sync Start • Data Type = 11 0001 (31h) H Sync End

In order to represent timing information as accurately as possible a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Similarly, a V Sync End event implies an H Sync Start event for the last line of the VSA..

Sync events should occur in pairs, Sync Start and Sync End, if accurate 1054 pulse-length information needs to be conveyed. Alternatively, if only a single point (event) in time is required, a single sync event (normally, Sync Start) may be transmitted to the peripheral. Sync events may be concatenated with blanking packets to

convey inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Note there is a power penalty for keeping the data line in HS mode, however. Display modules that do not need traditional sync/blanking/pixel timing should transmit pixel data in a high-speed burst then put the bus in Low Power Mode, for reduced power consumption. The recommended burst size is a scan line of pixels, which may be temporarily stored in a line buffer on the display module.

- Color Mode On Command, and, Data Type = 01 0010 (12h)

Color Mode On is a Short packet command that switches a Video Mode display module to 8-colors mode for power saving.

- Color Mode Off Command, Data Type = 00 0010 (02h)

Color Mode Off is a Short packet command that returns a Video Mode display module from 8-colors mode to normal display operation.

- Shutdown Peripheral Command, Data Type = 10 0010 (22h)

Shutdown Peripheral command is a Short packet command that turns off the display in a Video Mode display module for power saving. Note the interface shall remain powered in order to receive the turn-on, or wake-up, command.

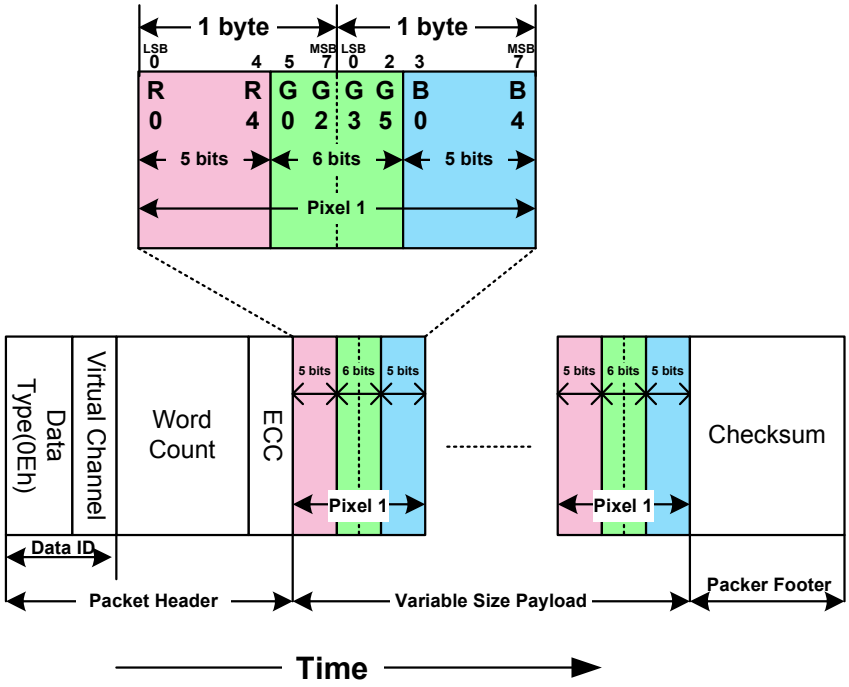
- Turn On Peripheral Command, Data Type = 11 0010 (32h)

Turn On Peripheral command is Short packet command that turns on the display in a Video Mode display module for normal display operation.

- Blanking Packet (Long), Data Type = 01 1001 (19h)

A Blanking packet is used to convey blanking timing information in a Long packet. Normally, the packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have Sync Event packets interspersed between blanking segments. Like all packets, the Blanking packet contents shall be an integer number of bytes. Blanking packets may contain arbitrary data as payload. The Blanking packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes, and a two-byte checksum.

- Packed Pixel Stream, 16-bit Format, Long packet, Data Type = 00 1110 (0Eh)



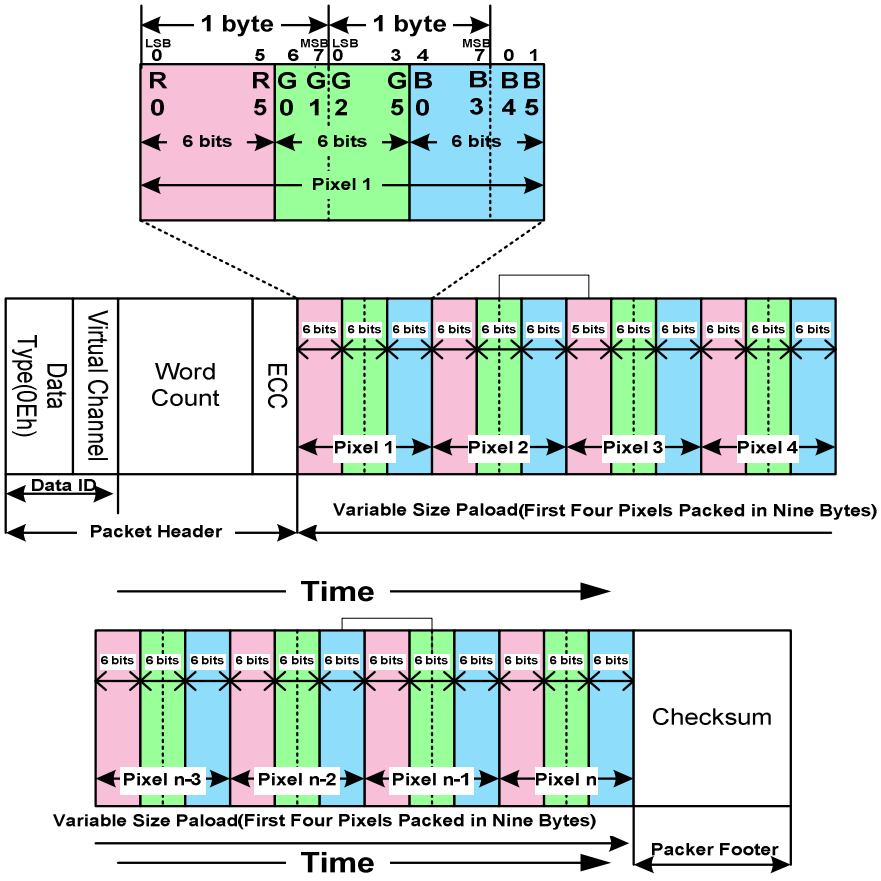
16-bit per Pixel-RGB Color Format, Long packet

Packed Pixel Stream 16-Bit Format is a Long packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is five bits red, six bits green, five bits blue, in that order. Note that the “Green” component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

Normally, the display module has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifacts.

- Packed Pixel Stream, 18-bit Format, Long packet, Data type = 01 1110 (1Eh)



18-bit per Pixel-RGB Color Format, Long pack

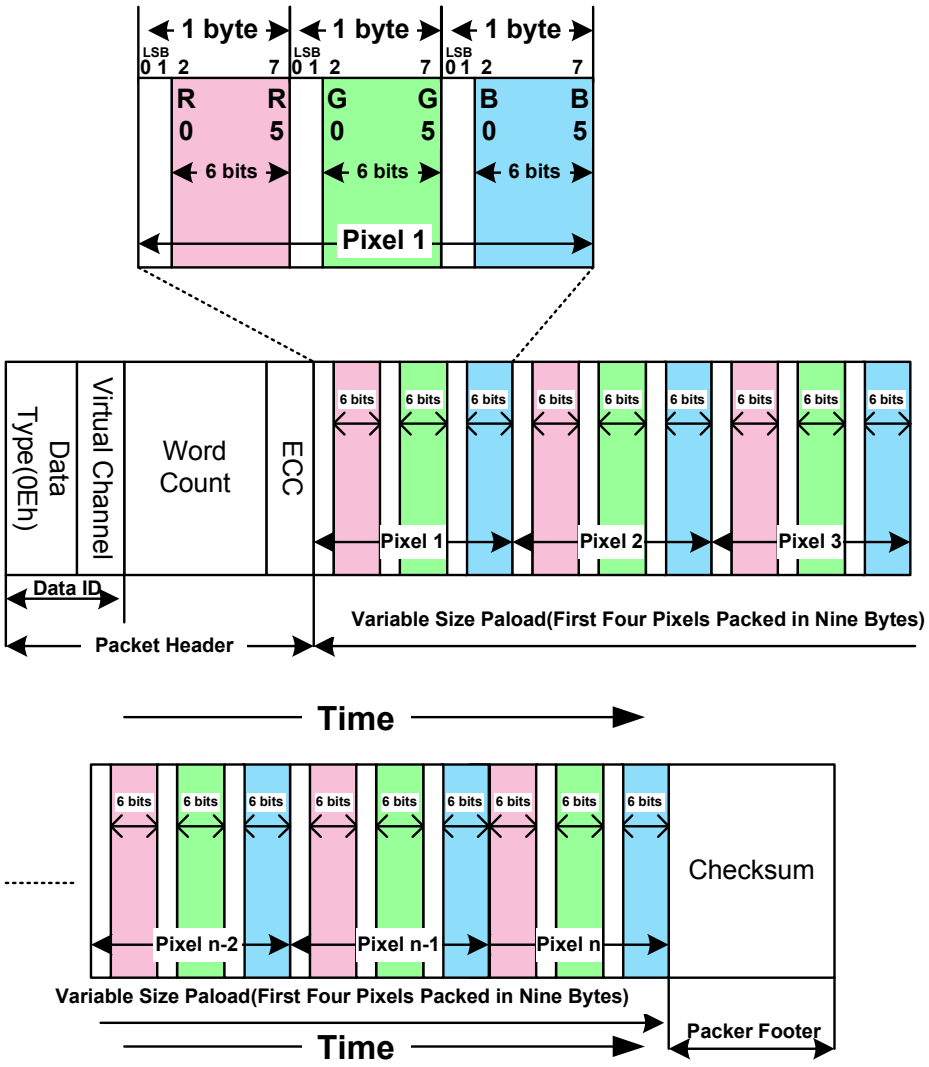
Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the fill pixels when refreshing the display device.

For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission.

With this format, the total line width (displayed plus non-displayed pixels) should be a multiple of four pixels (nine bytes).

- Pixel Stream, 18-bit Format in Three Bytes, Long packet, Data Type = 101110 (2Eh)



18-bit per Pixel (Loosely Packed)-RGB Color Format, Long pack

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the Link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

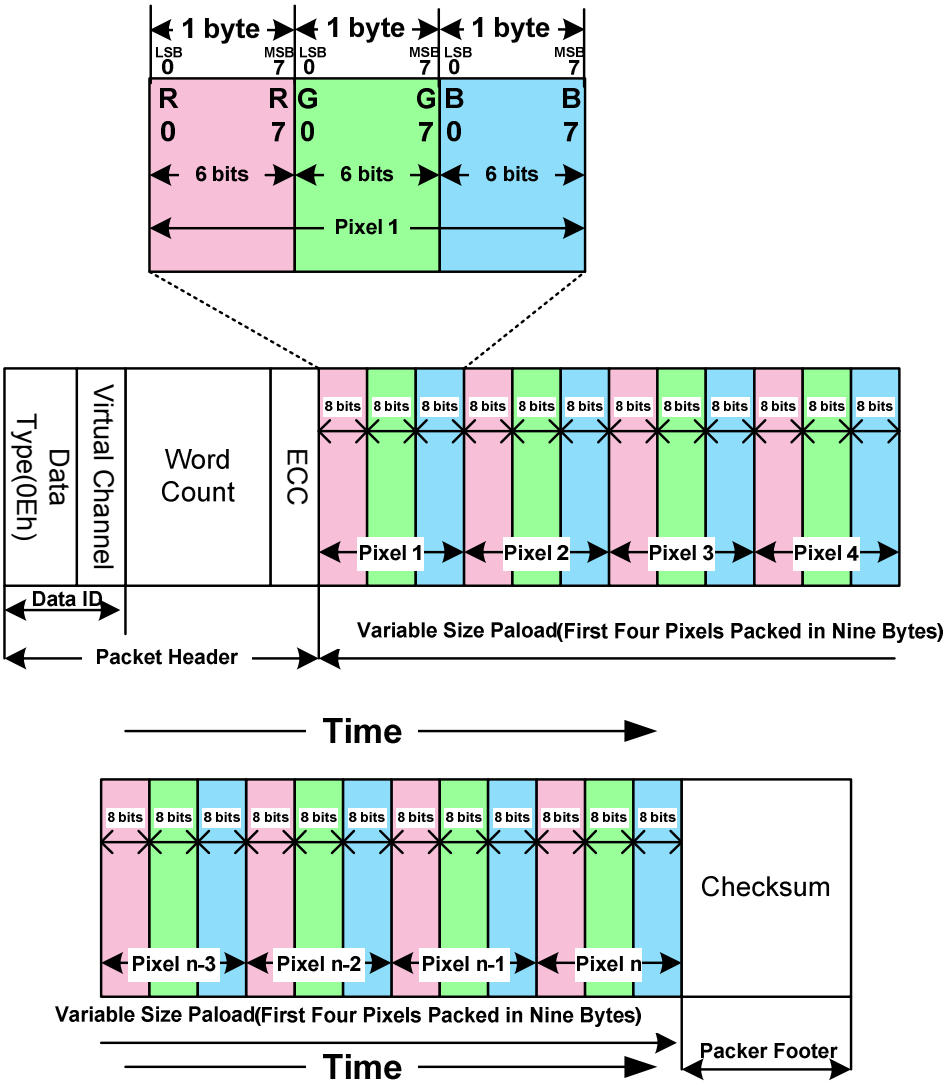
This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

- Packed Pixel Stream, 24-bit Format, Long packet, Data Type = 11 1110 (3Eh)

Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.



24-bit per Pixel -RGB Color Format, Long packet

8.3.2 Packet from the Display Module To The MCU

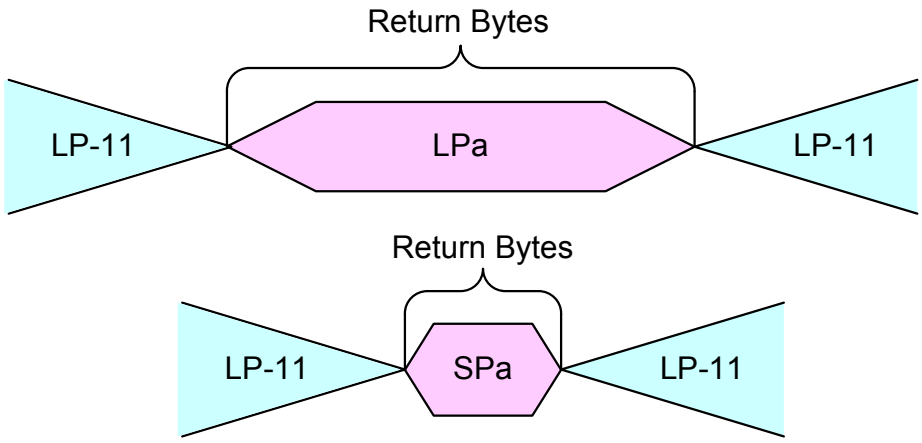
- Used Packet Types

The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) Read, No Parameter",(DCSRN-S)) or an Acknowledge with Error Report .The used packet type is defined on Data Type (DT)..

A number of the return bytes are more than the maximum size of the Packet Data (PD) on Long Packet (LPa) or Short Packet (SPa) when the display module is sending return bytes in several packets until all return bytes have been sent from the display module to the MCU.

It is not possible that the display module is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent on a packet.

Both cases are illustrated for reference purposes below.



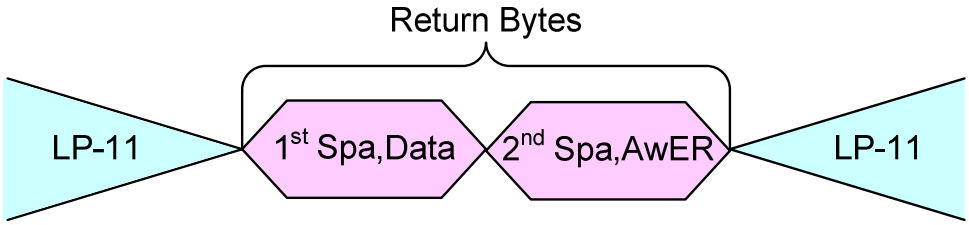
Return Bytes on Signal Packet

Data Type Hex	Data Type Binary	Symbol	Description	Packet Size
02h	00 0010	AwER	Acknowledge & Error Report	Short
1Ch	01 1100	DCSRR-L	DCS Long Read Response	Long
21h	10 0001	SCSRR1-S	DCS Short Read Response, 1 Byte returned	Short
22h	01 0010	DCSRR2-S	DCS Short Read Response, 2 Byte returned	Short
1Ah	01 1010	GENRR-L	Generic Long Read Response	Long
11h	01 0001	GENRR1-S	Generic Long Read Response, 1 Byte returned	Short
12h	01 0010	GENRR2-S	Generic Long Read Response, 2 Byte returned	Short

Data Type for Display Module-sourced Packets

The display module is return 2 packets (1st packet: Data, 2nd packet Acknowledge with Error Report) to the MCU when the display module has received a read command. See section "Display Command Set (DCS)

Read, No Parameter (DCSRN-S)" where has been detected and corrected a single bit error by the EEC (See bit 8 on Table" Acknowledge with Error Report (AwER) for Short Packet (SPa) Response"). This return packets are illustrated for reference purpose below.



Exception When Return Bytes on Several Packet

AwER=Acknowledge with Error Report

- Acknowledge with Error Report (AwER), Data Type = 00 0010(02h)

"Acknowledge with Error Report" (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT,00 0010b), from the display module to the MCU.

The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to '1',as they are defined on the following table.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to '0' internally
15	DSI Protocol Violation

Acknowledge with Error Report (AwER) for Long Packet (LPa) Response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Set to “0” internally (Only for Long Packet (LP))
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to ‘0’ internally
15	DSI Protocol Violation

Acknowledge with Error Report (AwER) for Short Packet (SPa) Response

These errors are only included on the last packet, which has been received from the MCU to the display module before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors

Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 00 0010b

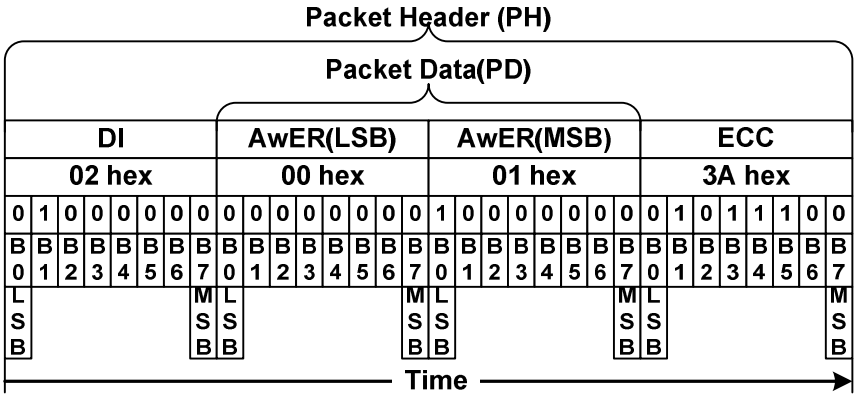
• Packet Data (PD):

  • Bit 8: ECC Error, single-bit (detected and corrected)

  • AwER: 0100h

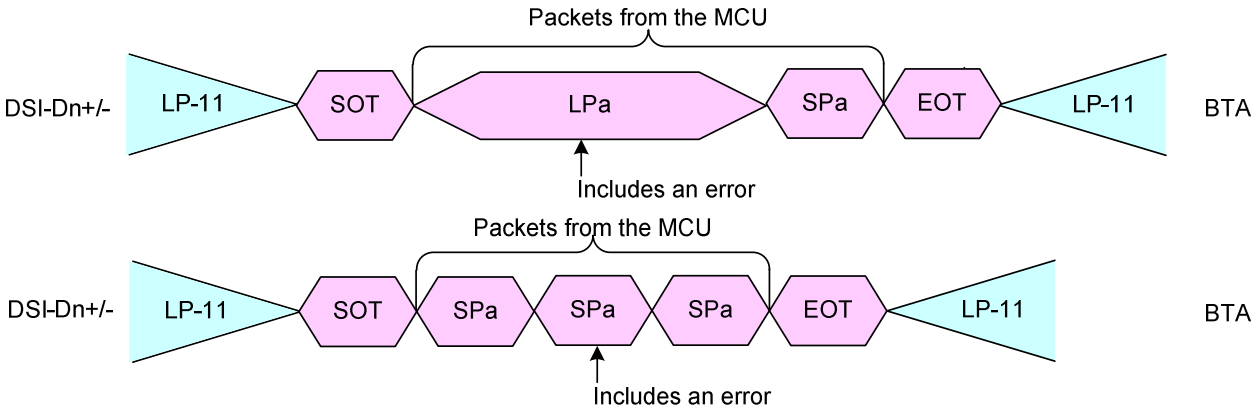
• Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Acknowledge with Error Report (AwER)-Example

It is possible that the display module receivers several packets, which include error, from the MPU before the MPU performs the Bus Turnaround (BTA).Some examples are illustrated below for reference purpose.



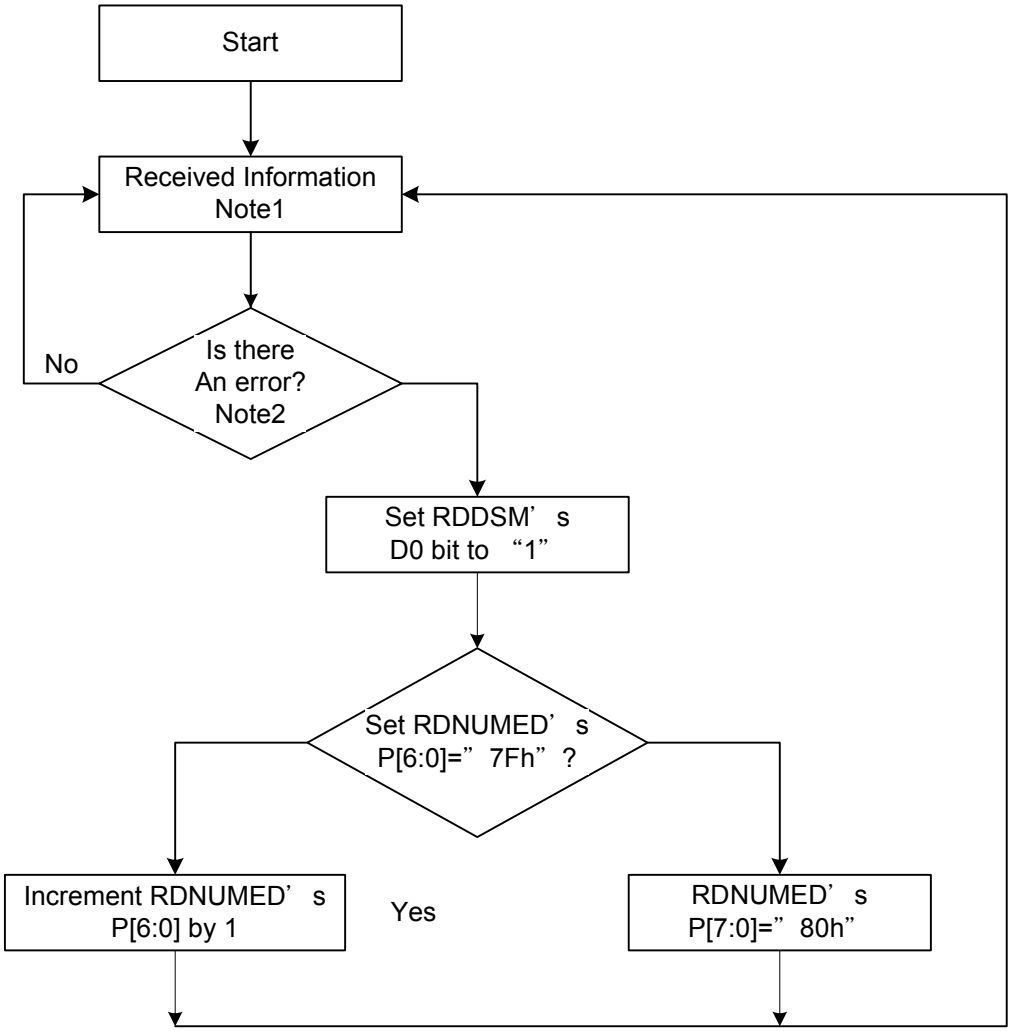
Error Packet

Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)”commands.

The bit D0 of the “Read Display Signal Mode (0Eh)” command has been set to ‘1’ if a received packet includes an error.

The number of the packets, which are including an ECC or CRC error, are calculated on the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h as well as set the bit D0 of the “Read Display Signal Mode (0Eh)” command to ‘0’ after the MCU has read the RDNUMED register from the display module.

The functionality of the RDNUMED register is illustrated for reference purposes below.



Notes:

1. This information can Interface or Packet Level Communication but it is always from the MCU to the display module in this case.

2. CRC or ECC err

- DCS Read Long Response (DCSRR-L), Data Type = 01 1100(1Ch)

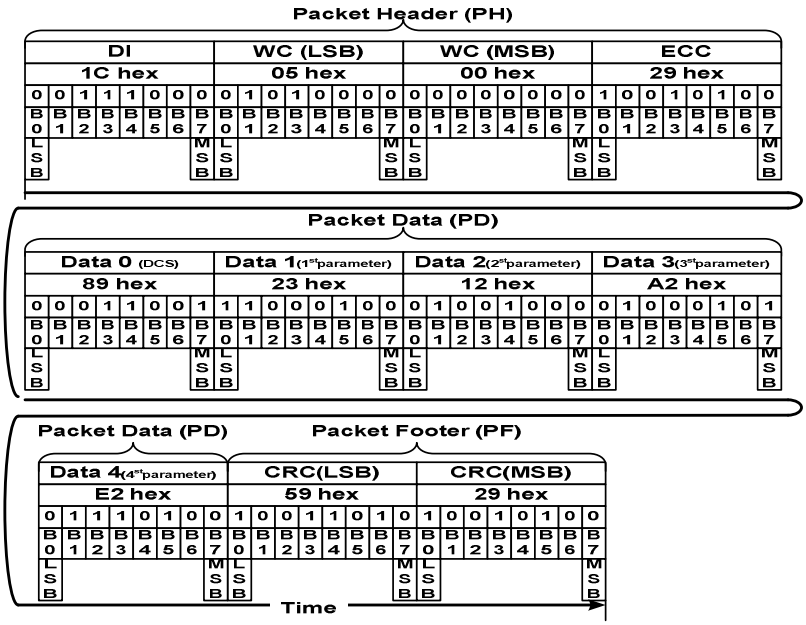
"DCS Read Long Response" (DCSRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT,01 1100b), from the display module to the MCU. "DCS Read Long Response" (DCSRR-L) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

"DCS Read Long Response" (DCSRR-L) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

• Data Identification (DI)
  • Virtual Channel (VC, DI[7…6]): 00b
  • Data Type (DT, DI[5…0]): 01 1100b
• Word Count (WC)
  • Word Count (WC): 0005h
• Error Correction Code (ECC)
• Packet Data (PD):
  • Data 0: 89h
  • Data 1: 23h
  • Data 2: 12h
  • Data 3: A2h
  • Data 4: E2h
• Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.



DCS Read Long Response(DCSRR-L)-Example

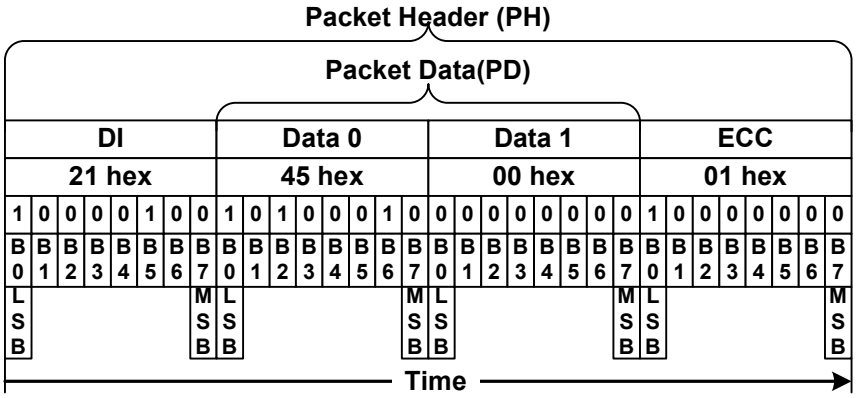
- DCS Read Short Response, 1 Byte Returned (DCSRR1-S), Data Type = 10 0001(21h)

"DCS Read Short Response, 1 Byte Returned" (DCSRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0001b), from the display module to the MCU. "DCS Read Short Response, 1 Byte Returned" (DCSRR1-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

• Data Identification (DI)
  • Virtual Channel (VC, DI[7…6]): 00b
  • Data Type (DT, DI[5…0]): 10 0001b
• Packet Data (PD):
  • Data 0: 45h
  • Data 1: 00h (Always)
• Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.



DCS Read Short Response,1 Byte Returned(DCSRR1-S)-Example

- DCS Read Short Response, 2 Bytes Returned (DCSRR2-S), Data Type = 10 0010(22h)

"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0010b), from the display module to the MCU. "DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 10 0010b

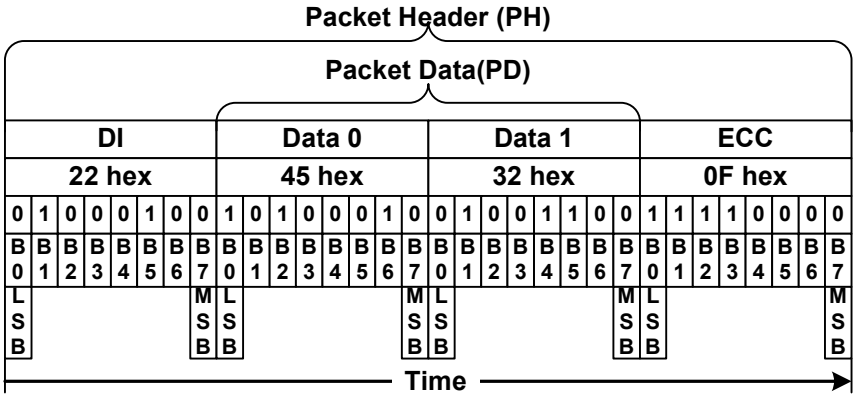
• Packet Data (PD):

  • Data 0: 45h

  • Data 1: 32h

• Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



DCS Read Short Response,2 Bytes Returned (DCSRR2-S) –Exampl

- Generic Read Long Response (GENRR-L), Data Type = 01 1010(1Ah)

"Generic Read Long Response" (GENRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 01 1010b), from the display module to the MCU. "Generic Read Long Response" (GENRR-L) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module.

Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 01 1010b

• Word Count (WC)

• Word Count (WC): 0005h

• Error Correction Code (ECC)

• Packet Data (PD):

  • Data 0: 89h

  • Data 1: 23h

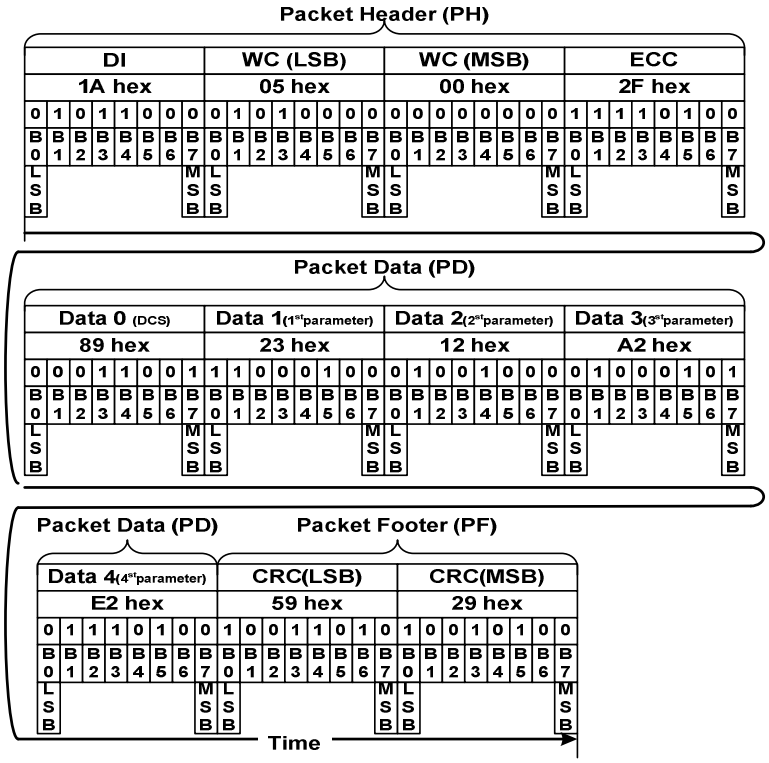
  • Data 2: 12h

  • Data 3: A2h

  • Data 4: E2h

• Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.



- Generic Read Short Response, 1 Byte Returned (GENRR1-S), Data Type = 01 0001(11h)

“Generic Read Short Response, 1 Byte Returned” (GENRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0001b), from the display module to the MCU. “Generic Read Short Response, 1Byte Returned” (GENRR1-S) is used when the display module wants to response a Generic Read command,

which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

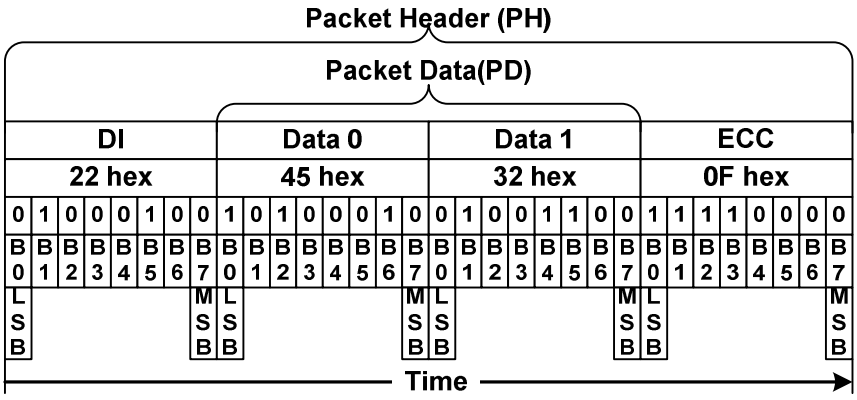
  • Data Type (DT, DI[5…0]): 01 0001b

• Packet Data (PD):

- Data 0: 45h
- Data 1: 00h (Always)

• Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.



Generic Read Short Response,1 Byte Returned (GENRR1-S)-Example

- Generic Read Short Response, 2 Bytes Returned (GENRR2-S), Data Type = 01 0010(12h)

"Generic Read Short Response, 2 Bytes Returned" (GENRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0010b), from the display module to the MCU. "Generic Read Short Response, 2Bytes Returned" (GENRR2-S) is used when the display module wants to response a Generic Read command,

which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

• Data Identification (DI)

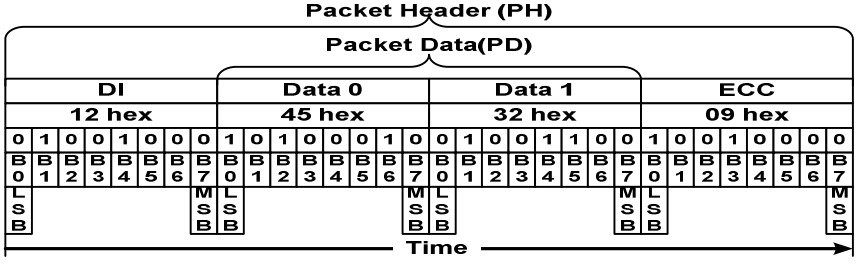
- Virtual Channel (VC, DI[7…6]): 00b
- Data Type (DT, DI[5…0]): 01 0010b

• Packet Data (PD):

- Data 0: 45h
- Data 1: 32h

• Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.



8.4. Communication Sequences

8.4.1 General

The communication sequences can be done on interface or packet levels between the MCU and the display module. See chapters “Interface Level Communication” and “Packet Level Communication”.

This communication sequence description is for DSI data lanes and it has been assumed that the needed low level communication is done on DSI clock lanes (DSI-CLK+/-) automatically.

Functions of the interface level communication is described on the following table.

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop state
	LPDT	Low power data transmission
	ULPS	Ultra-Low power state
	RAR	Remote application reset
	TEE	Tearing effect event
	ACK	Acknowledge (No error)
	BTA	Bus turnaround
High Speed	HSDT	High speed data transmission

Interface Level Communication

Functions of the packet level communication are described on the following table.

Packet Sender	Abbreviation	Packet Size	Packet Description
MCU	DCSW1-S	SPa	DCS Write,1 Parameter
	DCSWN-S	SPa	DCS Write, No parameter
	DCSW-L	LPa	DCS Write,Long
	DCSRN-S	SPa	DCS Read,No Parameter
	SMRPS-S	SPa	Set maximum return packet size
	NP-L	LPa	Null packet, No data
Display Module	AwER	SPa	Acknowledge with error report
	DCSRR-L	LPa	DCS Read, Long Response
	DCSRR1-S	SPa	DCS Read, Short Response
	DCSRR2-S	SPa	DCS Read, Short Response

Packet Level Communication

8.4.2 Sequences

- DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” is defined on chapter

"Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)" and example sequences, how this packet is used,is described on following tables.

DCS Write,1 Parameter Sequence – Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	LPDT	=>	-	-	-
3	-	LP-11	=>	-	-	End

DCS Write,1 Parmeter Sequence – Example2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	-
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

DCS Write, 1 Parameter Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	-
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	-
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error=>goto line8 If error=goto line 13
7	-	-	-	-	-	-
8	-	-	<=	ACK	-	No error
9	-	-	<=	LP-11	-	-
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	End
12	-	-	-	-	-	-
13	-	-	<=	LPDT	AwER	Error report
14	-	-	<=	LP-11	-	-
15	-	BTA	<=>	BTA	-	-
16	-	LP-11	=>	-	-	End

- DCS Write, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” is defined on chapter“Display Command Set (DCS) Write, No Parameter (DCSWN-S)” and example sequences, how this packet is used, is described on following tables.

DCS Write,No Parameter Sequence-Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	LPDT	=>	-	-	-
3	-	LP-11	=>	-	-	End

DCS Write,No Parmeter Sequence – Example2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	-
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

DCS Write, No Parameter Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	-
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	-
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error=>goto line8 If error=goto line 13
7	-	-	-	-	-	-
8	-	-	<=	ACK	-	No error
9	-	-	<=	LP-11	-	-
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	End
12	-	-	-	-	-	-
13	-	-	<=	LPDT	AwER	Error report

14	-	-	<=	LP-11	-	-
15	-	BTA	<=>	BTA	-	-
16	-	LP-11	=>	-	-	End

- DCS Write Long Sequence

A Long Packet (LPa) of “Display Command Set (DCS) Write Long (DCSW-L)” is defined on chapter “Display Command Set (DCS) Write Long (DCSW-L)” and example sequences, how this packet is used, is described on following tables.

DCS Write, Long Sequence-Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	LPDT	=>	-	-	-
3	-	LP-11	=>	-	-	End

DCS Write, Long Sequence – Example2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	-
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

DCS Write, Long Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	-
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	-
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error=>goto line8 If error=goto line 13
7	-	-	-	-	-	-
8	-	-	<=	ACK	-	No error
9	-	-	<=	LP-11	-	-
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU

11	-	LP-11	=>	-	-	End
12	-	-	-	-	-	-
13	-	-	<=	LPDT	AwER	Error report
14	-	-	<=	LP-11	-	-
15	-	BTA	<=>	BTA	-	-
16	-	LP-11	=>	-	-	End

- DCS Read, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” is defined on chapter“Display Command Set (DCS) Read, No Parameter (DCSRN-S)” and example sequences, how this packet is used, is described on following tables.

DCS Read, No Parameter Sequence – Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	SMRPS-S	HSDT	=>	-	-	Define how many data byte is wanted to read: 1 byte
3	DCSRN-S	HSDT	=>	-	-	Wanted to get a response ID1 (DAh)
4	EoTP	HSDT	=>	-	-	End of Transmission Packet
5	-	LP-11	=>	-	-	-
6	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
7	-	-	<=	LP-11	-	If no error=>goto line 9 If error=> goto line 14 If error is corrected by ECC =>go to line 19
8	-	-	-	-	-	-
9	-	-	<=	LPDT	DCSRR1-S	Responsed 1 byte return
10	-	-	<=	LP-11	-	-
11	-	BTA	<=>	BTA	-	Interface control change from the Display module to the MCU
12	-	LP-11	=>	-	-	End
13	-	-	-	-	-	-
14	-	-	<=	LPDT	AwER	Error report
15	-	-	<=	LP-11	-	-
16	-	BTA	<=>	BTA	-	Interface Control change from the Display module to the MCU
17	-	LP-11	=>	-	-	End
18	-	-	-	-	-	-
19	-	-	<=	LPDT	DCSRR1-S	Responsed 1 byte return
20	-	-	<=	LPDT	AwER	Error Report (Error is Corrected by ECC)

21	-	-	<=	LP-11	-	-
22	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
23	-	LP-11	=>	-	-	End

- Null Packet, No Data Sequence

A Long Packet (LPa) of “Null Packet, No Data (NP-L)” is defined on chapter “Null Packet, No Data (NP-L)” and example sequences, how this packet is used, is described on following tables.

Null Packet, No Parameter Sequence - Example

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	NP-L	HSDT	=>	-	-	Only high speed data transmission Is used
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

- End of Transmission Packet

A Short Packet (SPa) of “End of Transmission (EoT)” is defined on chapter “End of Transmission Packet (EoT)”and an example sequences, how this packet is used, is described on following tables.

End of Transmission Packet – Example

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	NP-L	HSDT	=>	-	-	Only high speed data transmission Is used
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

8.4.3 Video Mode Communication

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing ofDSI traffic for this type of display module.

8.4.3.1 Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. In the following sections, Burst Mode refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:

• Non-Burst Mode with Sync Pulses – enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.

• Non-Burst Mode with Sync Events – similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.

• Burst mode – RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral. To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. It is recommended to return to LP state once per scan-line during the horizontal blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or become, zero, and burst mode will be indistinguishable from non-burst mode.

During the BLLP the DSI Link may do any of the following:

• Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX

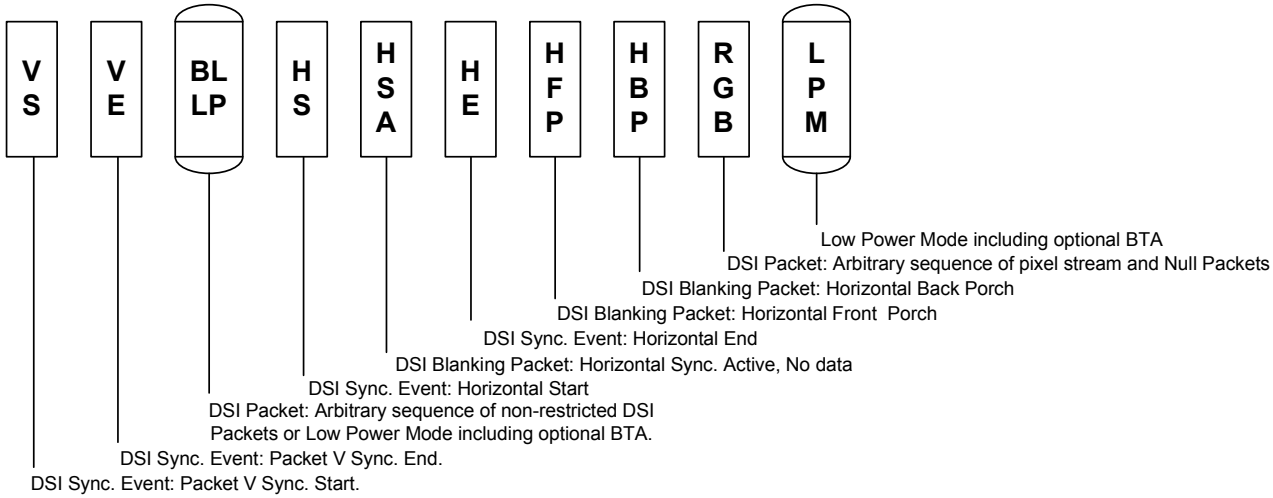
• Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode

• Transmit one or more non-video packets from the host processor to the peripheral using HS Mode

• If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode

• Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VS; all other lines shall start with HS. This is also true in the special case when VSA+VBP=0. Note that the position of synchronization packets, such as VS and HS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel. Normally, RGB pixel data is sent with one full scan line of pixels in a single packet. If necessary, a horizontal scan-line of active pixels may be divided into two or more packets. However, individual pixels shall not be split across packets.

Transmission packet components used in the figures in this section are defined in Figure below unless otherwise specified.



DSI Video Mode Interface Timing Legend

If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

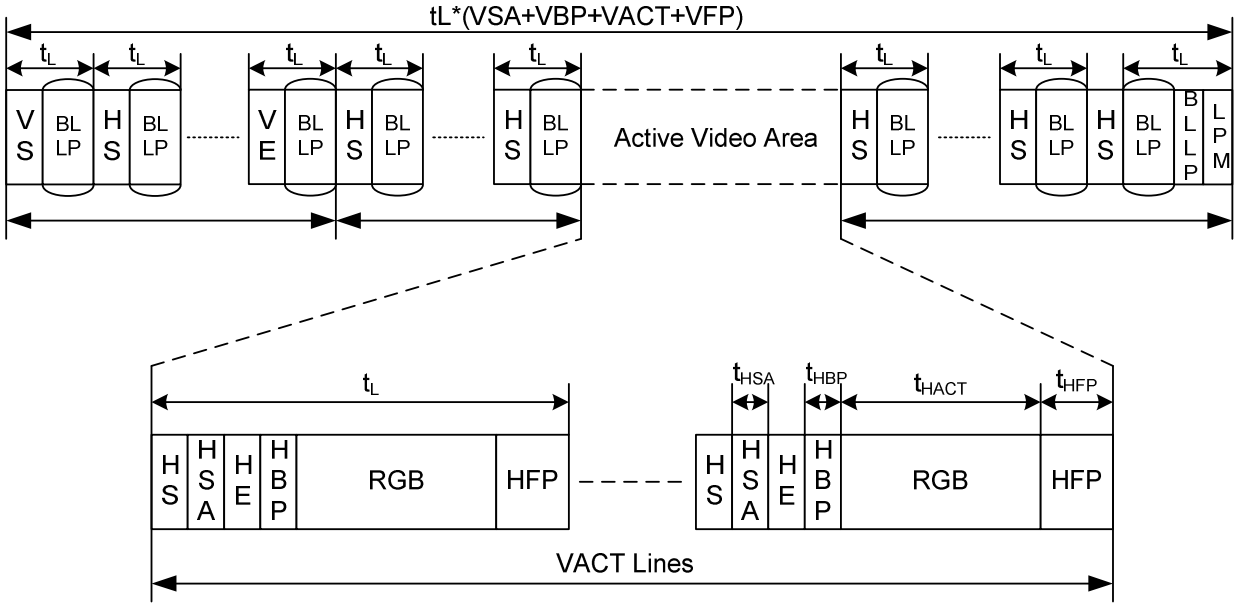
There are two limitation for MIPI Video mode 2 Lane:

(1) The packet number for H-porch or 1-line data should be even.

(2) Packet Pixel Stream should be start at Lane0.

8.4.3.2 Non-Burst Mode With Sync Pulses

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure below.



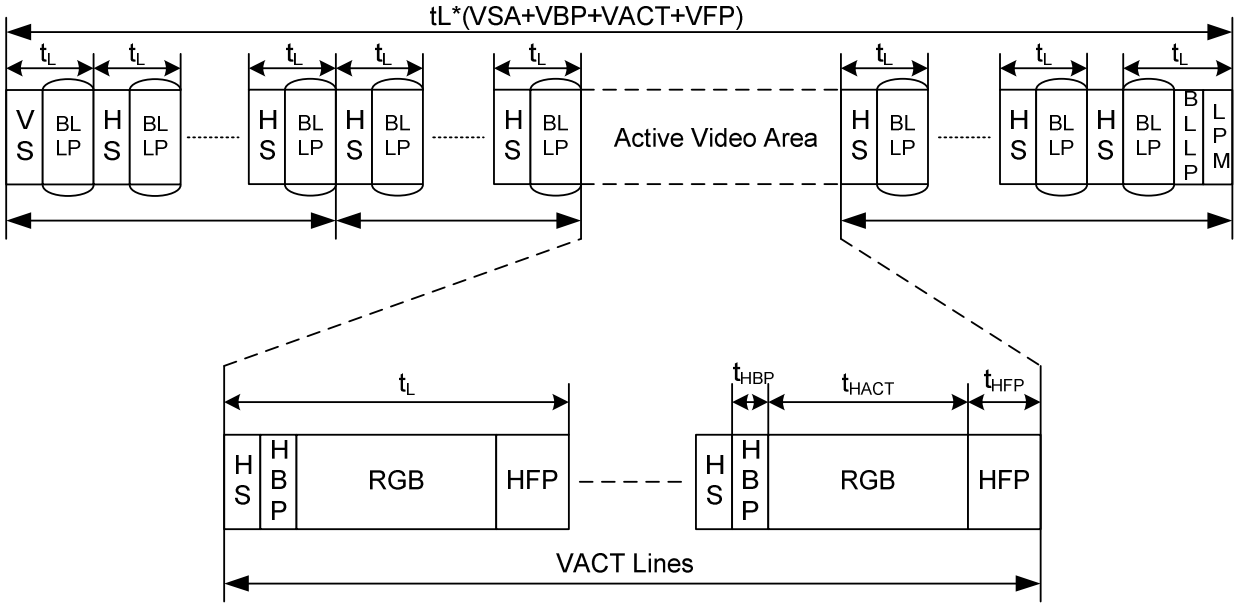
DSI Video Mode Interface Timing: Non-Burst Transmission with Sync Start and End

Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

8.4.3.3 Non-Burst Mode

This mode is a simplification of the format described in section 5.3.2.4.2 "Non-Burst Mode with Sync Pulse" .Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. Pixels are transmitted at the same rate as they would in a corresponding parallel display interface such as DPI-2.

An example of this mode is shown in Figure below.



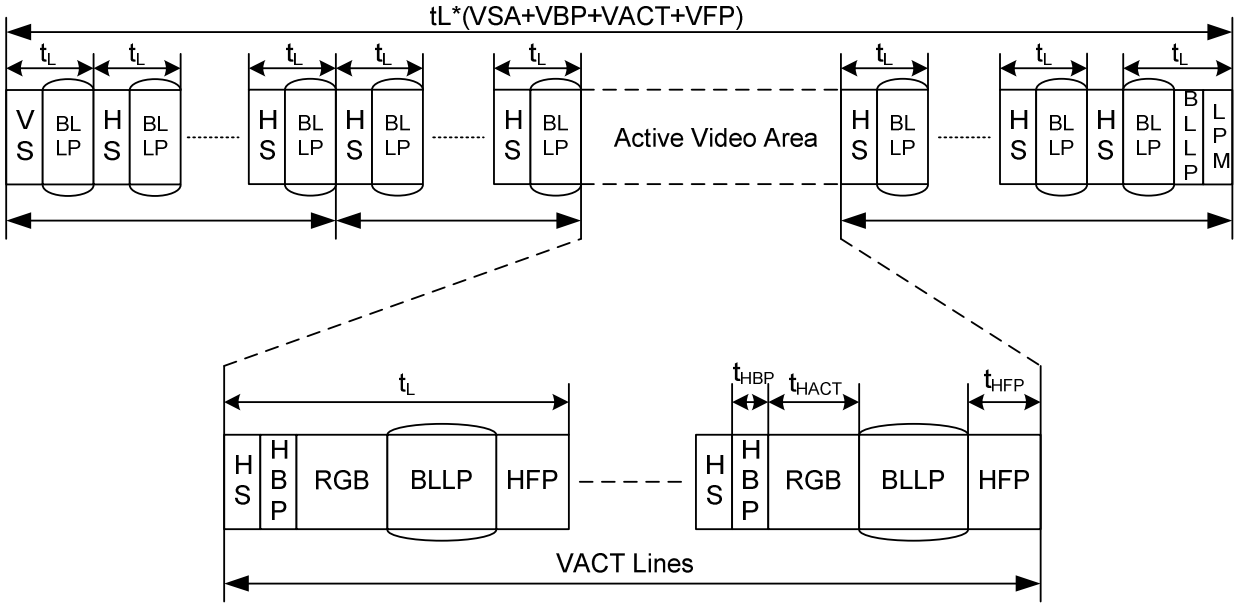
DSI Video Mode Interface Timing: Non-burst Transmission

As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again,a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

8.4.3.4 Burst Mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction. There may be a line buffer or similar memory on the peripheral to accommodate incoming data at high speed. Following HS pixel data transmission, the bus goes to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device.

An example of this mode is shown in Figure below.



DSI Video Mode Interface Timing: Burst Transmission

Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again,a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

9. POWER DEFINITION

9.1. Power Level

5 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 16.7M colors.

2. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display area is used but with 8 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display area is used but with 2 colors.

4. Sleep In Mode

In this mode, the DC: DC converter, internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VCI power supply. Contents of the memory are safe.

5. Power Off Mode

In this mode, both VCI and VDDI are removed.

Note: Transition between modes 1-4 is controllable by MIPI commands. Mode 6 is entered only when both Power supplies are removed.

9.2.. Power ON/OFF Sequence

VDDI and VCI can be applied in any order.

VCI and VDDI can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VCI can be powered down minimum 0msec after RESX has been released.

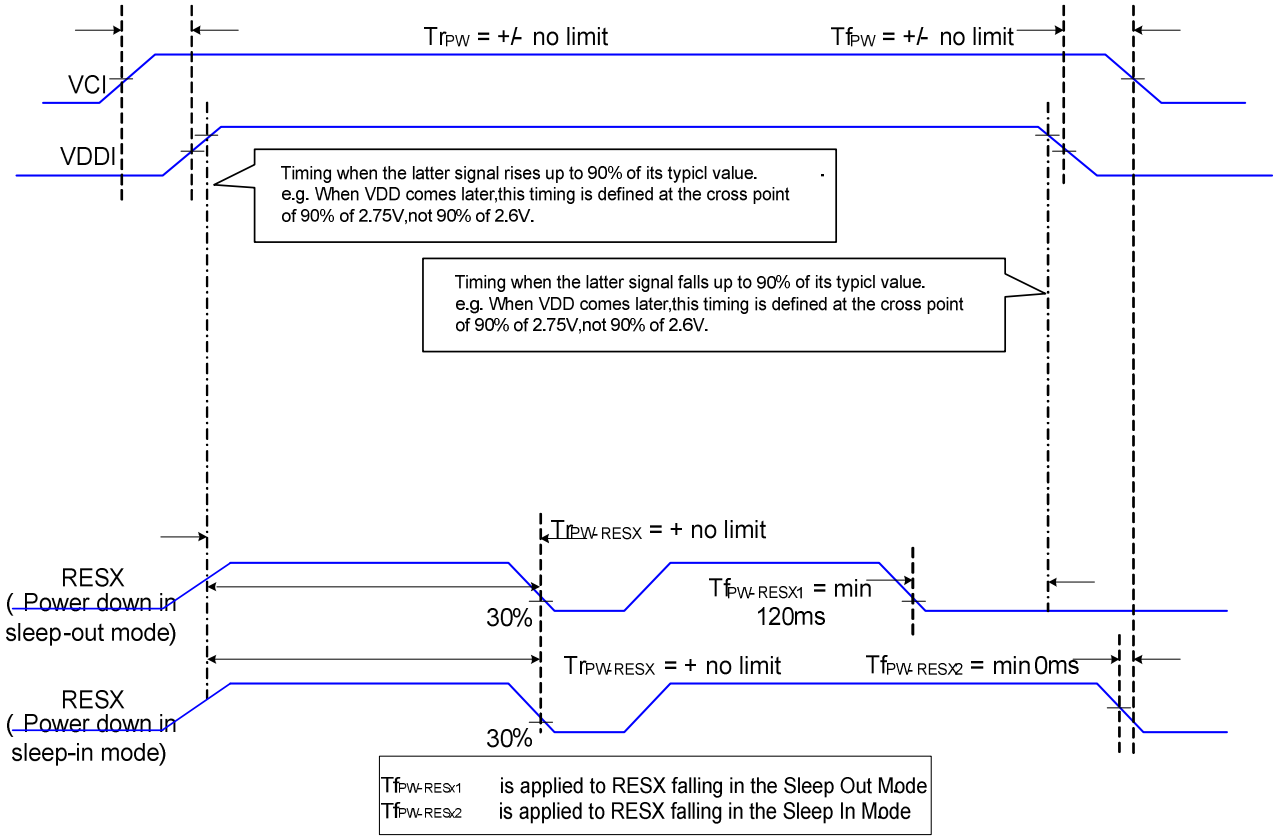
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below

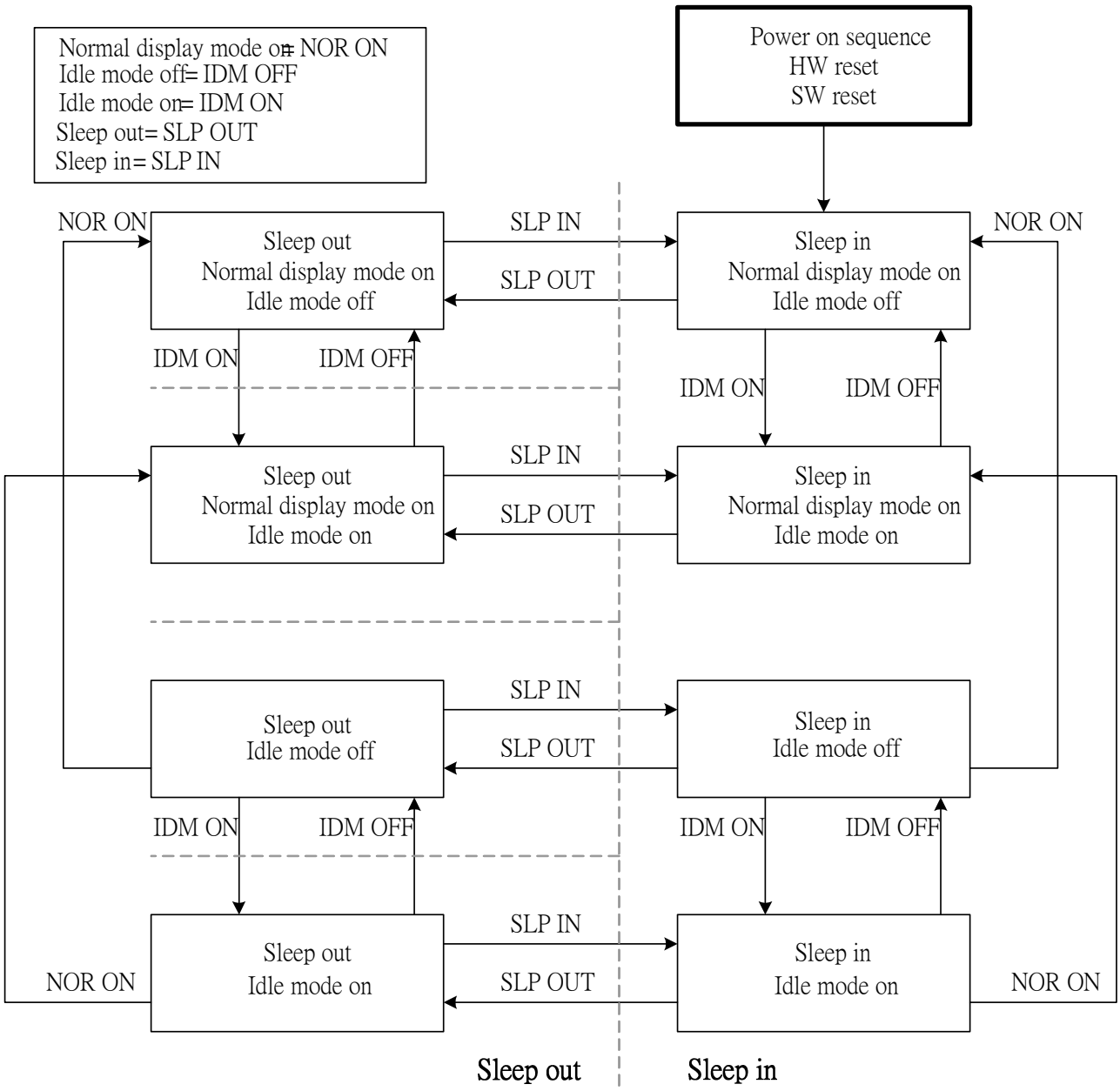


9.3.. Uncontrolled Power OFF

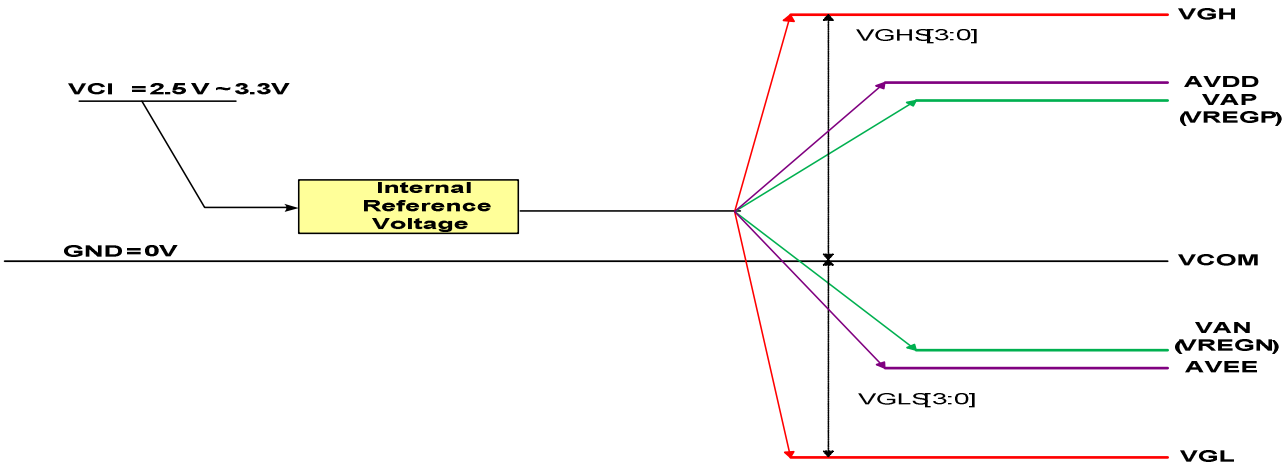
The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until “Power On Sequence” powers it up.

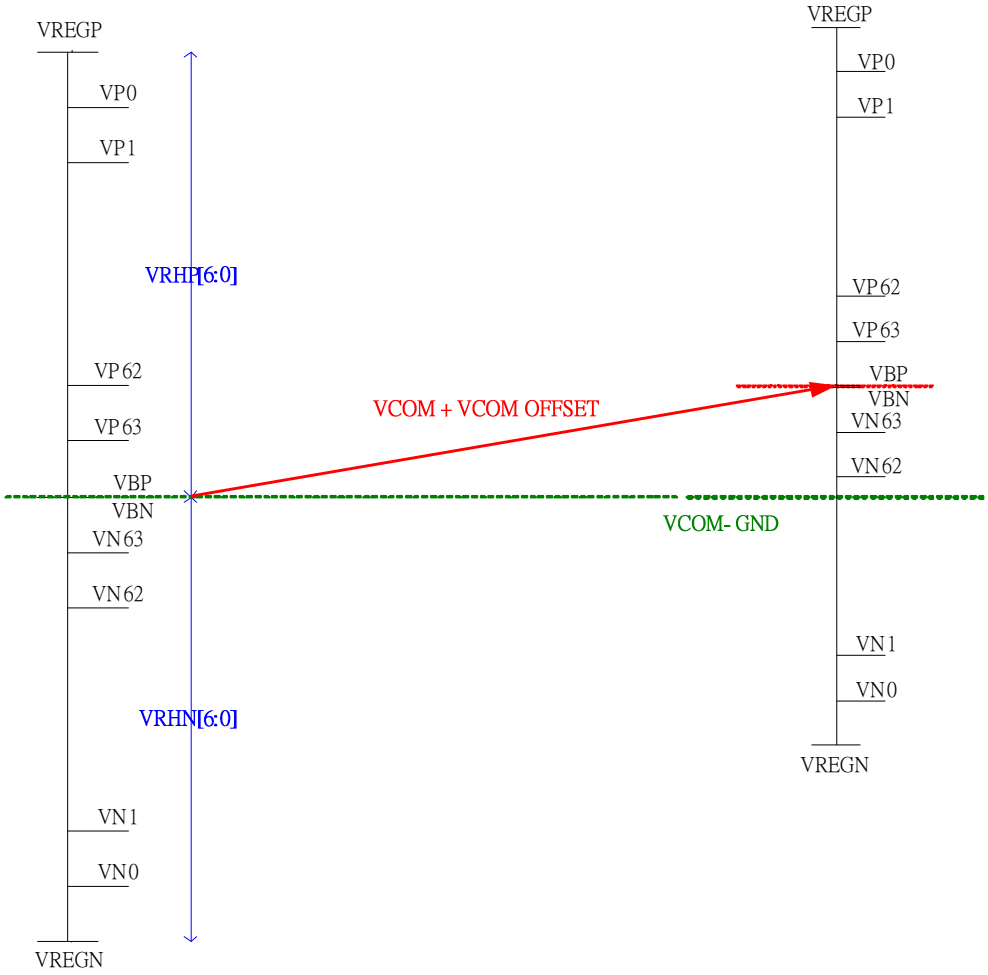
9.4.. Power Flow Chart



9.5.. Voltage Generation



9.6.. Relationship about source voltage



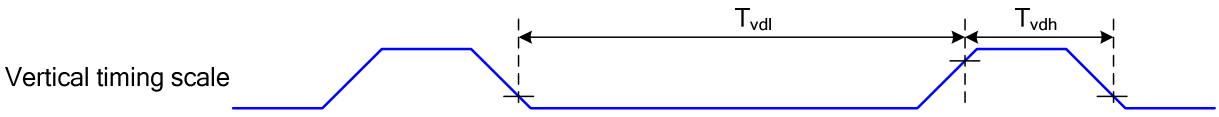
10. FUNCTION DESCRIPTION

10.1. Tearing Effect

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

10.1.1 Tearing effect line modes

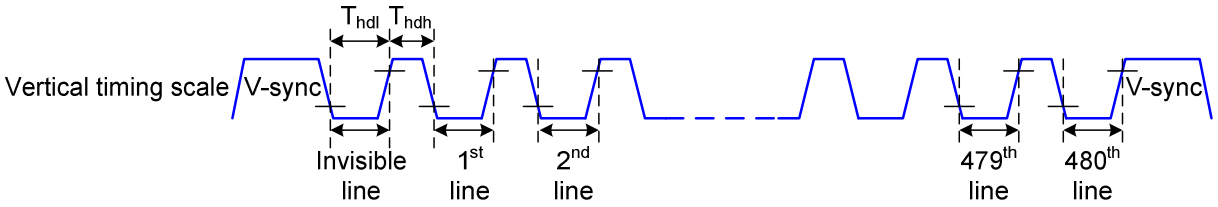
Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



tvdh= The LCD display is not updated from the Frame Memory

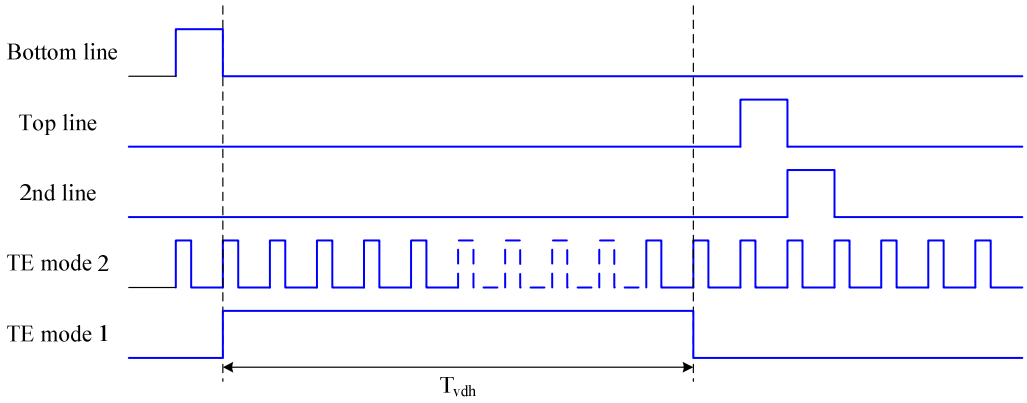
tvdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 400 H-sync pulses per field.



thdh= The LCD display is not updated from the Frame Memory

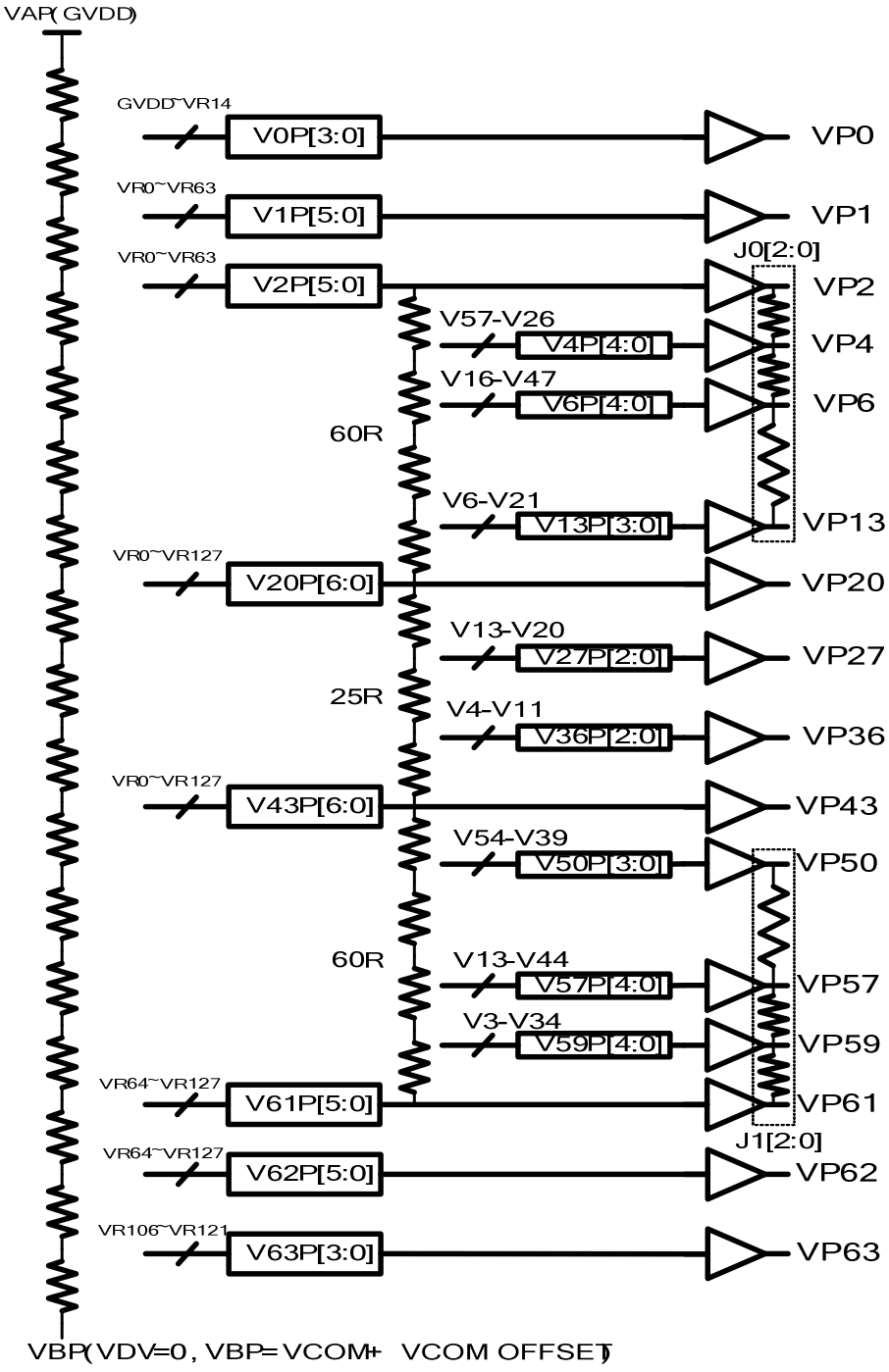
thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)



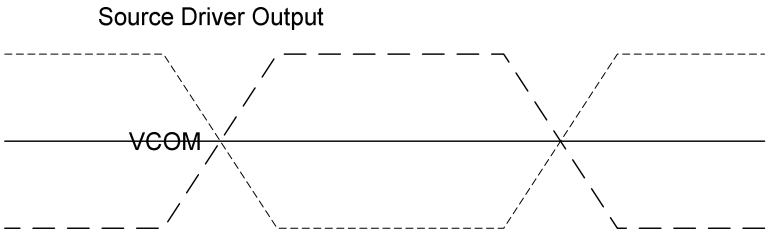
Note: During Sleep In Mode, the Tearing Output Pin is active Low.

10.2. Gamma Correction

ST7797 incorporate the gamma correction function to display 16.7M colors for the LCD panel. The gamma correction is performed with 3 groups of registers, which are gradient adjustment, contrast adjustment and fine- adjustment registers for positive and negative polarities, and RGB can be adjusted individually.



Gray scale Voltage Generation (Positive)



Relationship between Source Output and VCOM

Percentage adjustment:

VJ0P[2:0], VJ1P[2:0], VJ0N[2:0], VJ1N[2:0] these register are used to adjust the voltage level of interpolation point. The following table is the detail description.

VJ0P[2:0]/VJ0N[2:0]:

	00h	01h	02h	03h	04h	05h	06h	07h
VP3/VN3	50%,18	56%,20	50%,18	60%,22	42%,15	65%,23	45%,16	70%,25
VP5/VN5	50%,18	44%,16	50%,18	42%,15	65%,23	52%,19	40%,14	33%,12
VP7/VN7	86%,30	71%,25	80%,28	66%,23	88%,31	70%,25	76%,27	60%,21
VP8/VN8	71%,25	57%,20	63%,22	49%,17	61%,21	52%,18	58%,20	46%,16
VP9/VN9	57%,20	40%,14	49%,17	34%,12	60%,21	41%,15	47%,16	30%,11
VP10/VN10	43%,15	29%,10	34%,12	23%,8	46%,16	25%,9	36%,13	20%,7
VP11/VN11	29%,10	17%,6	20%,7	14%,5	32%,11	26%,9	23%,8	12%,4
VP12/VN12	14%,5	6%,2	9%,3	6%,2	20%,7	11%,4	17%,6	3%,1

VJ1P[2:0]/VJ1N[2:0]:

	00h	01h	02h	03h	04h	05h	06h	07h
VP51/VN51	86%,30	86%,30	86%,30	89%,31	77%,27	92%,32	83%,29	95%,33
VP52/VN52	71%,25	71%,25	77%,27	80%,28	63%,22	69%,24	75%,26	83%,29
VP53/VN53	57%,20	60%,21	63%,22	69%,24	48%,17	54%,19	66%,23	72%,25
VP54/VN54	43%,15	46%,16	46%,16	51%,18	35%,12	41%,14	55%,19	60%,21
VP55/VN55	29%,10	34%,12	31%,11	37%,13	23%,8	40%,14	26%,9	43%,15
VP56/VN56	14%,5	17%,6	14%,5	20%,7	9%,3	23%,8	11%,4	26%,9
VP58/VN58	50%,18	56%,20	47%,17	47%,17	53%,19	59%,21	45%,16	42%,15
VP60/VN60	50%,18	50%,18	50%,18	53%,19	42%,15	45%,16	55%,20	60%,21

voltage level percentage adjustment description

Source voltage of positive gamma level

Gamma level	Related Register	Formula
VP0	V0P[3:0]	(VAP-VBP)*(129R-V0P[3:0]R)/129R+VBP
VP1	V1P[5:0]	(VAP-VBP)*(128R-V1P[5:0]R)/129R+VBP
VP2	V2P[5:0]	(VAP-VBP)*(128R-V2P[5:0]R)/129R+VBP
VP3	VJ0P[2:0]	(VP2-VP4)* VJ0P[2:0]+VP4
VP4	V4P[4:0]	(VP2-VP20)*(57R-V4P[4:0])/60R+VP20
VP5	VJ0P[2:0]	(VP4-VP6)* VJ0P[2:0]+VP6
VP6	V6P[4:0]	(VP2-VP20)*(47R-V6P[4:0])/60R+VP20
VP7	VJ0P[2:0]	(VP6-VP13)* VJ0P[2:0]+VP13
VP8	VJ0P[2:0]	(VP6-VP13)* VJ0P[2:0]+VP13
VP9	VJ0P[2:0]	(VP6-VP13)* VJ0P[2:0]+VP13
VP10	VJ0P[2:0]	(VP6-VP13)* VJ0P[2:0]+VP13
VP11	VJ0P[2:0]	(VP6-VP13)* VJ0P[2:0]+VP13
VP12	VJ0P[2:0]	(VP6-VP13)* VJ0P[2:0]+VP13
VP13	V13P[3:0]	(VP2-VP20)*(21R-V13P[3:0])/60R+VP20
VP14	--	(VP13-VP20)/(20-13)*(20-14)+VP20
VP15	--	(VP13-VP20)/(20-13)*(20-15)+VP20
VP16	--	(VP13-VP20)/(20-13)*(20-16)+VP20
VP17	--	(VP13-VP20)/(20-13)*(20-17)+VP20
VP18	--	(VP13-VP20)/(20-13)*(20-18)+VP20
VP19	--	(VP13-VP20)/(20-13)*(20-19)+VP20
VP20	V20P[6:0]	(VAP-VBP)*(128R-V20P[6:0]R)/129R+VBP
VP21	--	(VP20-VP27)/(27-20)*(27-21)+VP27
VP22	--	(VP20-VP27)/(27-20)*(27-22)+VP27
VP23	--	(VP20-VP27)/(27-20)*(27-23)+VP27
VP24	--	(VP20-VP27)/(27-20)*(27-24)+VP27
VP25	--	(VP20-VP27)/(27-20)*(27-25)+VP27
VP26	--	(VP20-VP27)/(27-20)*(27-26)+VP27
VP27	V27P[2:0]	(VP20-VP43)*(20R-V27P[2:0])/25R+VP43
VP28	--	(VP27-VP36)/(36-27)*(36-28)+VP36
VP29	--	(VP27-VP36)/(36-27)*(36-29)+VP36
VP30	--	(VP27-VP36)/(36-27)*(36-30)+VP36
VP31	--	(VP27-VP36)/(36-27)*(36-31)+VP36
VP32	--	(VP27-VP36)/(36-27)*(36-32)+VP36
VP33	--	(VP27-VP36)/(36-27)*(36-33)+VP36
VP34	--	(VP27-VP36)/(36-27)*(36-34)+VP36
VP35	--	(VP27-VP36)/(36-27)*(36-35)+VP36
VP36	V36P[2:0]	(VP20-VP43)*(11R-V36P[2:0])/25R+VP43
VP37	--	(VP36-VP43)/(43-36)*(43-37)+VP43
VP38	--	(VP36-VP43)/(43-36)*(43-38)+VP43
VP39	--	(VP36-VP43)/(43-36)*(43-39)+VP43
VP40	--	(VP36-VP43)/(43-36)*(43-40)+VP43
VP41	--	(VP36-VP43)/(43-36)*(43-41)+VP43
VP42	--	(VP36-VP43)/(43-36)*(43-42)+VP43
VP43	V43P[6:0]	(VAP-VBP)*(128R-V43P[6:0]R)/129R+VBP
VP44	--	(VP43-VP50)/(50-43)*(50-44)+VP50
VP45	--	(VP43-VP50)/(50-43)*(50-45)+VP50
VP46	--	(VP43-VP50)/(50-43)*(50-46)+VP50
VP47	--	(VP43-VP50)/(50-43)*(50-47)+VP50
VP48	--	(VP43-VP50)/(50-43)*(50-48)+VP50
VP49	--	(VP43-VP50)/(50-43)*(50-49)+VP50
VP50	V50P[3:0]	(VP43-VP61)*(54R-V50P[3:0])/60R+VP61
VP51	VJ1P[2:0]	(V5P0-VP57)*VJ1P[2:0]+VP57

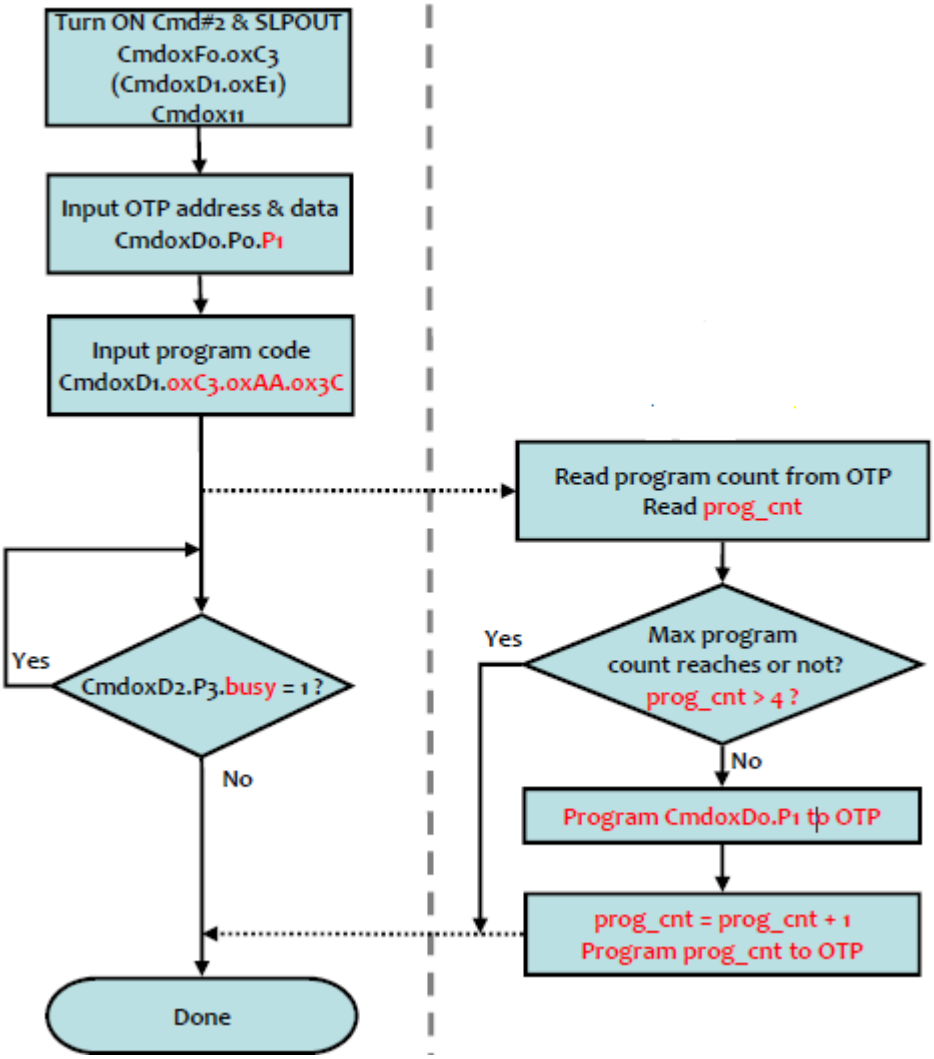
VP52	VJ1P[2:0]	(VP50-VP57)* VJ1P[2:0]+VP57
VP53	VJ1P[2:0]	(VP50-VP57)* VJ1P[2:0]+VP57
VP54	VJ1P[2:0]	(VP50-VP57)* VJ1P[2:0]+VP57
VP55	VJ1P[2:0]	(VP50-VP57)* VJ1P[2:0]+VP57
VP56	VJ1P[2:0]	(VP50-VP57)* VJ1P[2:0]+VP57
VP57	V57P[4:0]	(VP43-VP61)*(44R-V57P[4:0])/60R+VP61
VP58	VJ1P[2:0]	(VP57-VP59)* VJ1P[2:0]+VP59
VP59	V59P[4:0]	(VP43-VP61)*(34R-V59P[4:0])/60R+VP61
VP60	VJ1P[2:0]	(VP59-VP61)* VJ1P[2:0]+VP61
VP61	V61P[5:0]	(VAP-VBP)*(64R-V61P[5:0]R)/129R+VBP
VP62	V62P[5:0]	(VAP-VBP)*(64R-V62P[5:0]R)/129R+VBP
VP63	V63P[3:0]	(VAP-VBP)*(23R-V63P[3:0]R)/129R+VBP

Source voltage of negative gamma level

Gamma level	Related Register	Formula
VN0	V0N[3:0]	VBN-(VBN-VAN)*(129R-V0N[3:0]R)/129R
VN1	V1N[5:0]	VBN-(VBN-VAN)*(128R-V1N[5:0]R)/129R
VN2	V2N[5:0]	VBN-(VBN-VAN)*(128R-V2N[5:0]R)/129R
VN3	VJ0N[2:0]	(VN2-VN4)*VJ0N[2:0]+VN4
VN4	V4N[4:0]	(VN2-VN20)*(57R-V4N[4:0])/60R+VN20
VN5	VJ0N[2:0]	(VN4-VN6)* VJ0N[2:0]+VN6
VN6	V6N[4:0]	(VN2-VN20)*(47R-V6N[4:0])/60R+VN20
VN7	VJ0N[2:0]	(VN6-VN13)* VJ0N[2:0]+VN13
VN8	VJ0N[2:0]	(VN6-VN13)* VJ0N[2:0]+VN13
VN9	VJ0N[2:0]	(VN6-VN13)* VJ0N[2:0]+VN13
VN10	VJ0N[2:0]	(VN6-VN13)* VJ0N[2:0]+VN13
VN11	VJ0N[2:0]	(VN6-VN13)* VJ0N[2:0]+VN13
VN12	VJ0N[2:0]	(VN6-VN13)* VJ0N[2:0]+VN13
VN13	V13N[3:0]	(VN2-VN20)*(21R-V13N[3:0])/60R+VN20
VN14	--	(VN13-VN20)/(20-13)*(20-14)+VN20
VN15	--	(VN13-VN20)/(20-13)*(20-15)+VN20
VN16	--	(VN13-VN20)/(20-13)*(20-16)+VN20
VN17	--	(VN13-VN20)/(20-13)*(20-17)+VN20
VN18	--	(VN13-VN20)/(20-13)*(20-18)+VN20
VN19	--	(VN13-VN20)/(20-13)*(20-19)+VN20
VN20	V20N[6:0]	VBN-(VBN-VAN)*(128R-V20N[6:0]R)/129R
VN21	--	(VN20-VN27)/(27-20)*(27-21)+VN27
VN22	--	(VN20-VN27)/(27-20)*(27-22)+VN27
VN23	--	(VN20-VN27)/(27-20)*(27-23)+VN27
VN24	--	(VN20-VN27)/(27-20)*(27-24)+VN27
VN25	--	(VN20-VN27)/(27-20)*(27-25)+VN27
VN26	--	(VN20-VN27)/(27-20)*(27-26)+VN27
VN27	V27N[2:0]	(VN20-VN43)*(20R-V27N[2:0])/25R+VN43
VN28	--	(VN27-VN36)/(36-27)*(36-28)+VN36
VN29	--	(VN27-VN36)/(36-27)*(36-29)+VN36
VN30	--	(VN27-VN36)/(36-27)*(36-30)+VN36
VN31	--	(VN27-VN36)/(36-27)*(36-31)+VN36
VN32	--	(VN27-VN36)/(36-27)*(36-32)+VN36
VN33	--	(VN27-VN36)/(36-27)*(36-33)+VN36
VN34	--	(VN27-VN36)/(36-27)*(36-34)+VN36
VN35	--	(VN27-VN36)/(36-27)*(36-35)+VN36
VN36	V36N[2:0]	(VN20-VN43)*(11R-V36N[2:0])/25R+VN43
VN37	--	(VN36-VN43)/(43-36)*(43-37)+VN43

VN38	--	(VN36-VN43)/(43-36)*(43-38)+VN43
VN39	--	(VN36-VN43)/(43-36)*(43-39)+VN43
VN40	--	(VN36-VN43)/(43-36)*(43-40)+VN43
VN41	--	(VN36-VN43)/(43-36)*(43-41)+VN43
VN42	--	(VN36-VN43)/(43-36)*(43-42)+VN43
VN43	V43N[6:0]	VBN-(VBN-VAN)*(128R-V43N[6:0]R)/129R
VN44	--	(VN43-VN50)/(50-43)*(50-44)+VN50
VN45	--	(VN43-VN50)/(50-43)*(50-45)+VN50
VN46	--	(VN43-VN50)/(50-43)*(50-46)+VN50
VN47	--	(VN43-VN50)/(50-43)*(50-47)+VN50
VN48	--	(VN43-VN50)/(50-43)*(50-48)+VN50
VN49	--	(VN43-VN50)/(50-43)*(50-49)+VN50
VN50	V50N[3:0]	(VN43-VN61)*(54R-V50N[3:0])/60R+VN61
VN51	VJ1N[2:0]	(V5N0-VN57)*VJ1N[2:0]+VN57
VN52	VJ1N[2:0]	(VN50-VN57)* VJ1N[2:0]+VN57
VN53	VJ1N[2:0]	(VN50-VN57)* VJ1N[2:0]+VN57
VN54	VJ1N[2:0]	(VN50-VN57)* VJ1N[2:0]+VN57
VN55	VJ1N[2:0]	(VN50-VN57)* VJ1N[2:0]+VN57
VN56	VJ1N[2:0]	(VN50-VN57)* VJ1N[2:0]+VN57
VN57	V57N[4:0]	(VN43-VN61)*(44R-V57N[4:0])/60R+VN61
VN58	VJ1N[2:0]	(VN57-VN59)* VJ1N[2:0]+VN59
VN59	V59N[4:0]	(VN43-VN61)*(34R-V59N[4:0])/60R+VN61
VN60	VJ1N[2:0]	(VN59-VN61)* VJ1N[2:0]+VN61
VN61	V61N[5:0]	VBN-(VBN-VAN)*(64R-V61N[5:0]R)/129R
VN62	V62N[5:0]	VBN-(VBN-VAN)*(64R-V62N[5:0]R)/129R
VN63	V63N[3:0]	VBN-(VBN-VAN)*(23R-V63N[3:0]R)/129R

11 NVM PROGRAMMING FLOW



12 APPLICATION NOTE

12.1.. Layout Resistance Suggestion

Pin Name	Type	Maximum Resistance	
VDDI, VDDA, AGND, DGND	Power supply	10	Ω
VPP	Power supply	10	Ω
MIPI_CLK_P MIPI_CLK_N MIPI_DATA_P MIPI_DATA_N	MIPI	10	Ω
VCC, VCCM, MIPI_LDO, VGH, VGHS, VGL, SVDD, SVEE, AVDD, AVEE	Power supply	10	Ω
IMP, RESET, CSX, OSC, SCK	I	100	Ω
TE	O	100	Ω
SDA	I/O	100	Ω

13. COMMAND

13.1. Cmmand Table List

COMMAND Table 1														
Instruction	**D/CX**	**WRX**	**RDX**	**PNUM**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)	No operation
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)	Software reset
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)	Read display ID
	1	1	↑		ID1.7-0								(FFh)	ID1 read
	1	1	↑		ID2.7-0								(FFh)	ID2 read
	1	1	↑		ID3.7-0								(FFh)	ID3 read
Read Number of Errors on DSI	0	↑	1	-	0	0	0	0	0	1	0	1	(05h)	Read DSI
	1	1	↑		P.7-0								(00h)	
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)	Read display status
	1	1	↑		BSTON	0	0	0	ML	BGR	MH	0	(00h)	
	1	1	↑		0	DBI.2-0			IDMON	0	SLOUT	0	(60h)	
	1	1	↑		0	0	INVON	0	0	DISON	TEON	0	(00h)	
	1	1	↑		0	0	TEM	0	0	0	0	0	(00h)	
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)	Read display power
	1	1	↑		BSTON	IDMON	0	SLPOUT	0	DISON	0	0	(00h)	
RDD MADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)	Read display
	1	1	↑		0	0	0	ML	BGR	MH	0	0	(00h)	
RDD COLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)	Read display pixel format
	1	1	↑		0	0	0	0	0	DBI.2-0			(06h)	
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)	Read display image mode
	1	1	↑		-	0	INVON	0	0	0	0	0	(00h)	
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)	Read display signal mode
	1	1	↑		TEON	TEM	HSON	VSON	PCLKON	DEON	0	EOD	(00h)	
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)	Read display self-diagnostic result
	1	1	↑		RELD	FUND	0	0	0	0	0	CSCMP	(00h)	
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)	Sleep in
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)	Sleep out
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)	Display inversion off

COMMAND Table 1														
Instruction	**D/CX**	**WRX**	**RDX**	**PNUM**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)	Display inversion on
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)	Display off
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)	Display on
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)	Memory write
	1	↑	1		D1.7-0								-	
	1	↑	1		Dx.7-0								-	
	1	↑	1		Dn.7-0								-	
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)	Tearing effect off
TEON	0	↑	1	1	0	0	1	1	0	1	0	1	(35h)	Tearing effect on
	1	↑	1		-	-	-	-	-	-	-	M	(00h)	
MADCTL	0	↑	1	1	0	0	1	1	0	1	1	0	(36h)	Memory access control
	1	↑	1		-	-	-	ML	BGR	MH	-	-	(00h)	
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)	Idle mode off
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)	Idle mode on
COLMOD	0	↑	1	1	0	0	1	1	1	0	1	0	(3Ah)	Interface pixel format
	1	↑	1		-	-	-	-	-	DBI.2-0			(06h)	
RAMWRC	0	↑	1	-	0	0	1	1	1	1	0	0	(3Ch)	Memory write continue
	1	↑	1		D1.7-0								-	
	1	↑	1		Dx.7-0								-	
	1	↑	1		Dn.7-0								-	
TESLWR	0	↑	1	2	0	1	0	0	0	1	0	0	(44h)	Write tear scan line
	1	↑	1		-	-	-	-	-	-	-	N.8	(00h)	
	1	↑	1		N.7-0								(00h)	
TESLRD	0	↑	1	-	0	1	0	0	0	1	0	1	(45h)	Read scanline
	1	1	↑		-	-	-	-	-	-	-	N.8	(00h)	
	1	1	↑		N.7-0								(00h)	
WRIDMC	0	↑	1	1	1	0	0	1	0	0	0	0	(90h)	Write two-color idle mode
	1	↑	1		-	-	-	-	-	R	G	B	(07h)	
RDIDMC	0	↑	1	-	1	0	0	1	0	0	0	1	(91h)	Read two-color idle mode
	1	1	↑		-	-	-	-	-	R	G	B	(07h)	

COMMAND Table 1

Instruction	D/CX	WRX	RDX	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
RDFCHKSUM	0	↑	1	-	1	0	1	0	1	0	1	0	(AAh)	Read First Checksum
	1	1	↑		FCS.7-0								-	
RDCCHKSUM	0	↑	1	-	1	0	1	0	1	1	1	1	(AFh)	Read Continue Checksum
	1	1	↑		CCS.7-0								-	
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)	Read ID1
	1	1	↑		ID1.7-0								-	
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2
	1	1	↑		ID2.7-0								-	
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3
	1	1	↑		ID3.7-0								-	

COMMAND Table 2														
Instruction	**D/CX**	**WRX**	**RDX**	**PNUM**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
ECFC	0	↑	1	1	1	0	1	1	0	0	0	0	(B0h)	Entry Code Function
	1	↑	1		EC.7-0								(02h)	Control
FRC1	0	↑	1	2	1	0	1	1	0	0	0	1	(B1h)	Frame Rate Control 1
	1	↑	1		FRS.7-0								(FAh)	
	1	↑	1		RTN.7-0								(C6h)	
GSC	0	↑	1	1	1	0	1	1	0	0	1	0	(B2h)	Gate Scan Control
	1	↑	1					FGS	ML_GS_REV	GS.2-0			(10h)	
VDMDC	0	↑	1	1	1	0	1	1	0	0	1	1	(B3h)	Video Mode Display
	1	↑	1		-	-	-	-	DINV_A.3-0				(01h)	Control
TCMDC	0	↑	1	1	1	0	1	1	0	1	0	0	(B4h)	Two Color Mode Display
	1	↑	1		-	-	-	-	DINV_B.3-0				(01h)	Control
BPC	0	↑	1	4	1	0	1	1	0	1	0	1	(B5h)	Blank Porch Control
	1	↑	1		VFP.15-8								(00h)	
	1	↑	1		VFP.7-0								(02h)	
	1	↑	1		VBP.15-8								(00h)	
	1	↑	1		VBP.7-0								(03h)	
EMSET	0	↑	1	1	1	0	1	1	0	1	1	1	(B7h)	Entry Mode Set
	1	↑	1		-	-	-	-	DSTB	-	-	-	(00h)	
PWR1	0	↑	1	4	1	1	0	0	0	0	0	1	(C1h)	Power Control 1
	1	↑	1		VGHS2_A.3-0				VGHS1_A.3-0				(44h)	
	1	↑	1		-	-	-	-	VGLS_A.3-0				(06h)	
	1	↑	1		VPMS_A.3-0				VNMS_A.3-0				(ACh)	
	1	↑	1		-	-	VRH_A.5-0						(1Bh)	

COMMAND Table 2														
Instruction	**D/CX**	**WRX**	**RDX**	**PNUM**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
PWR2	0	↑	1	4	1	1	0	0	0	0	1	0	(C2h)	Power Control 2
	1	↑	1		VGHS2_B.3-0				VGHS1_B.3-0				(44h)	
	1	↑	1		-	-	-	-	VGLS_B.3-0				(06h)	
	1	↑	1		VPMS_B.3-0				VNMS_B.3-0				(ACh)	
	1	↑	1		-	-	VRH_B.5-0						(1Bh)	
VCOMCTL	0	↑	1	1	1	1	0	0	0	1	0	1	(C5h)	VCOM Control
	1	↑	1		VMF_MODE	VCOM.6-0							(57h)	

COMMAND Table 2														
Instruction	**D/CX**	**WRX**	**RDX**	**PNUM**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
PGC	0	↑	1	14	1	1	1	0	0	0	0	0	(E0h)	Positive Gamma Control
	1	↑	1		VC63P.3-0				VC0P.3-0				(F0h)	
	1	↑	1		-	-	VC1P.5-0						(03h)	
	1	↑	1		-	-	VC2P.5-0						(05h)	
	1	↑	1		-	-	-	VC4P.4-0					(09h)	
	1	↑	1		-	-	-	VC6P.4-0					(0Ch)	
	1	↑	1		-	VJ0P.2-0			VC13P.3-0				(0Fh)	
	1	↑	1		-	VC20P.6-0							(3Eh)	
	1	↑	1		-	VC36P.2-0			-	VC27P.2-0			(77h)	
	1	↑	1		-	VC43P.6-0							(4Fh)	
	1	↑	1		-	VJ1P.2-0			VC50P.3-0				(0Fh)	
	1	↑	1		-	-	-	VC57P.4-0					(17h)	
	1	↑	1		-	-	-	VC59P.4-0					(17h)	
	1	↑	1		-	-	VC61P.5-0						(21h)	
	1	↑	1		-	-	VC62P.5-0						(23h)	
NGC	0	↑	1		1	1	1	0	0	0	0	1	(E1h)	Negative Gamma Control
	1	↑	1		VC63N.3-0				VC0N.3-0				(F0h)	
	1	↑	1		-	-	VC1N.5-0						(03h)	
	1	↑	1		-	-	VC2N.5-0						(05h)	
	1	↑	1		-	-	-	VC4N.4-0					(09h)	
	1	↑	1		-	-	-	VC6N.4-0					(0Ch)	
	1	↑	1		-	VJ0N.2-0			VC13N.3-0				(0Fh)	
	1	↑	1		-	VC20N.6-0							(3Eh)	
	1	↑	1		-	VC36N.2-0			-	VC27N.2-0			(77h)	
	1	↑	1		-	VC43N.6-0							(4Fh)	
	1	↑	1		-	VJ1N.2-0			VC50N.3-0				(0Fh)	
	1	↑	1		-	-	-	VC57N.4-0					(17h)	
	1	↑	1		-	-	-	VC59N.4-0					(17h)	
	1	↑	1		-	-	VC61N.5-0						(21h)	
	1	↑	1		-	-	VC62N.5-0						(23h)	

COMMAND Table 3

Instruction	D/CX	WRX	RDX	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
DTRCON	0	↑	1	2	1	1	0	1	1	0	0	1	(D9h)	Dithering Control
	1	↑	1		EPF.1-0		EPFS	-	-	-	P24M.1-0		(00h)	
	1	↑	1		CEPM.1-0		MG.1-0		MB.1-0		MR.1-0		(95h)	
SRECON	0	↑	1	2	1	1	0	1	1	1	1	0	(DEh)	SRE Control
	1	↑	1		-	-	DRK.5-0						(00h)	
	1	↑	1		-	-	BRG.5-0						(00h)	
RLCMODE	0	↑	1	5	1	1	0	0	1	0	0	0	(C8h)	Run-length Control
	1	↑	1		BDHM	PPBS	BLANKSEL	POLARITY	BWSM.1-0		CTRM.1-0		(0Ch)	
	1	↑	1		-	-	-	-	RBNRTH.3-0				(08h)	
	1	↑	1		-	-	-	-	GBNRTH.3-0				(08h)	
	1	↑	1		-	-	-	-	BBNRTH.3-0				(08h)	
	1	↑	1		RLC_EC.7-0								(00h)	
MIPIMODE	0	↑	1	7	1	1	1	0	1	1	0	0	(ECh)	MIPI DPHY/DSI Control
	1	↑	1		F565	TXDIV2	ERPEN	EOTER_EN	ESCS_TREN	ESC_TREN	LPTX_TREN	HSRX_TREN	(00h)	
	1	↑	1		ESCS_TS.1-0		ESC_TS.1-0		LPTX_TS.1-0		HSRX_TS.1-0		(55h)	
	1	↑	1		EOTPER_EN	TOFRX_EN	DSK0.1-0		CSK.1-0		RJTC_EN	RJTA_EN	(00h)	
	1	↑	1		TAGETM	-	TAGETS.5-0						(00h)	
	1	↑	1		TAGOM	-	TAGOS.5-0						(00h)	
	1	↑	1		-	-	ERST_EN	SETIM	ENPDN	V1_2SET.2-0(VCCLP)			(08h)	
	1	↑	1		-	SETI2.2-0			-	SETI1.2-0			(33h)	

13.2. Cmmand Table 1

- NOP (00h)

00H	NOP (No Operation)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)
Parameter	No Parameter												-
Description	This command is empty command. "-" Don't care												
Restriction													
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart

- SWRESET (01h): Software Reset

01H	SWRESET (Software Reset)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)
Parameter	No Parameter												-
Description	"-" Don't care - When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. - Frame memory contents are unaffected by this command.												
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during this 5msec. If software reset is sent during sleep in mode, it will be necessary to wait 120msec before sending sleep out command.												

	Software reset command cannot be sent during sleep out sequence.

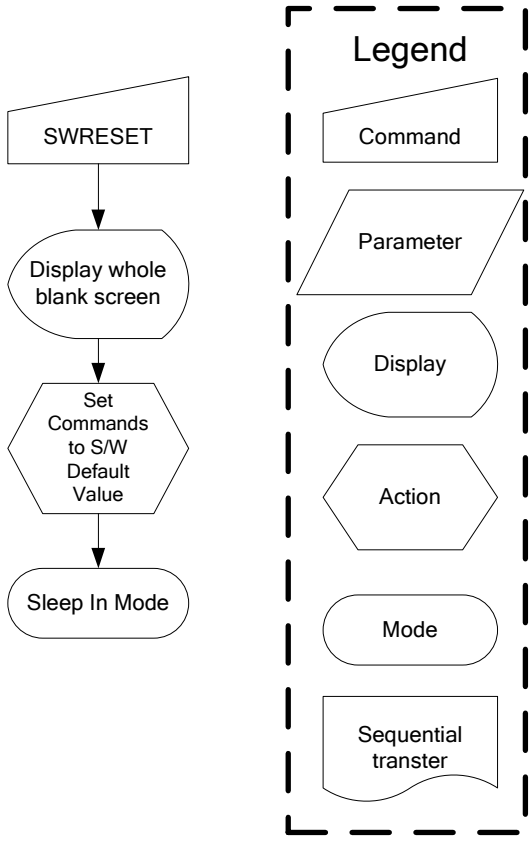
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart



- RDDID (04h): Read Display ID

04H	RDDID (Read Display ID)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)
1st parameter	1	1	↑	-	ID1.7-0								-
2nd parameter	1	1	↑	-	ID2.7-0								-
3rd parameter	1	1	↑	-	ID3.7-0								-
Description	- -The 1st parameter LCD module's manufacturer ID. -The 2nd parameter LCD module/driver version ID -The 3rd parameter LCD module/driver ID. -Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 1,2,3 of the command 04h, respectively. "-" Don't care												
Restriction													
Register availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	See description	See description	See description
S/W Reset	See description	See description	See description
H/W Reset	See description	See description	See description

- Read Number of the Errors on DSI (05h)

05H	RDNUMED (Read Number of the Errors on DSI)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	0	1	0	1	(05h)
parameter	1	1	↑	-	P.7-0								(00h)
Description	The first parameter is telling a number of the errors on DSI. The more detailed description of the bits is below. P[6..0] bits are telling a number of the errors. P[7] is set to '1' if there is overflow with P[6..0] bits. P[7..0] bits are set to '0's (as well as RDDSM(0Eh)'s D0 is set '0' at the same time) after there is sent the second parameter information (= The read function is completed). "-" Don't care												
Restriction	This command is available in MIPI interface. In the other interface, P[7:0] bits are set to "0"s.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

- RDDST (09h): Read Display Status

09H	RDDST (Read Display Status)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)
1st parameter	1	1	↑	-	BSTON	-	-	-	ML	BGR	MH	-	00-
2nd parameter	1	1	↑	-	-	DBI.2-0			IDMON	-	SLOUT	-	60
3rd parameter	1	1	↑	-	-	-	INVON	-	-	DISON	TEON	-	00
4th parameter	1	1	↑	-	-	-	TEM	-	-	-	-	-	00

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off
ML	Scan Address Order (ML)	'0' =Decrement, (LCD refresh Top to Bottom, when MADCTL (36h) D4='0') '1'=Increment, (LCD refresh Bottom to Top, when MADCTL (36h) D4='1')
BGR	RGB/ BGR Order (RGB)	'1' =BGR, (When MADCTL (36h) D3='1') '0' =RGB, (When MADCTL (36h) D3='0')
IDMON(D19)	Idle Mode On/Off	'1' = On, "0" = Off
SLPOUT(D17)	Sleep In/Out	'1' = Out, "0" = In
DBI.2-0	Display pixel input format for 1bpp mode	"101": 565 color; "110": 666 color; "111": 888 color
INVON(D13)	Inversion Status	'1' = On, "0" = Off
DISON(D10)	Display On/Off	'1' = On, "0" = Off
TEON(D9)	Tearing effect line on/off	'1' = On, "0" = Off
TEM(D5)	Tearing effect line mode	'0' = mode1, '1' = mode2

"-" Don't care

- RDDPM (0Ah): Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	-	(0Ah)
1st parameter	1	1	↑	-	BSTON	IDMON	-	SLPOUT	-	DISON	-	-	(00h)

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off
IDMON	Idle mode on/off	*'1' = Idle Mode On,* *'0' = Idle Mode Off*
SLPOUT	Sleep in/out	'1' =Sleep out, '0' =Sleep in,
DISON	Display on/off	'1' =Display on, '0' =Display off,

"-" Don't care

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000-1000(08h)
S/W Reset	0000-1000(08h)
H/W Reset	0000-1000(08h)

- RDDMADCTL (0Bh): Read Display MADCTL

0BH	RDDMADCTL (Read Display MADCTL)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDMADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)
1st parameter	1	1	↑	-	-	-	-	ML	RGB	MH	-	-	(00h)

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
ML	Scan Address Order (ML)	'0' =Decrement, (LCD refresh Top to Bottom, when MADCTL (36h) D4='0') '1'=Increment, (LCD refresh Bottom to Top, when MADCTL (36h) D4='1')
RGB	RGB/ BGR Order (RGB)	'1' =BGR, (When MADCTL (36h) D3='1') '0' =RGB, (When MADCTL (36h) D3='0')
MH	Horizontal Order	'0' =Decrement, (LCD refresh Left to Right, when MADCTL (36h) D2='0') '1' =Increment, (LCD refresh Right to Left, when MADCTL (36h) D2='1')
D1	Not used	'0'
D0	Not used	'0'

"-" Don't care

Restriction

There is one dummy parameter when using Parallel interface.

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000-0000 (00h)
S/W Reset	No change
H/W Reset	0000-0000 (00h)

- RDDCOLMOD (0Ch): Read Display Pixel Format

0CH	RDDCOLMOD (Read Display Pixel Format)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDCOLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)
1st parameter	1	1	↑	-	-	-	-	-	-	DBI.2-0			(06h)
Description	DBI.2-0: Display pixel input format for 1bpp mode. "101": 565 color; "110": 666 color; "111": 888 color. Others are no define and invalid "-" Don't care												
Restriction	There is one dummy parameter when using Parallel interface.												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000-0110 (18 bit/pixel)
S/W Reset	No change
H/W Reset	0000-0110 (18 bit/pixel)

- RDDIM (0Dh): Read Display Image Mode

0DH	RDDIM (Read Display Image Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)
1st parameter	1	1	↑	-	-	-	INVON	-	-	-	-	-	(00h)

Description

This command indicates the current status of the display as described in the table below:

-INVON: Inversion on/off

Gamma Curve Selection	GC2	GC1	GC0	Gamma set (26h) Parameter
Gamma curve 1	0	0	0	GC0
Gamma curve 2	0	0	1	GC1
Gamma curve 3	0	1	0	GC2
Gamma curve 4	0	1	1	GC3
Not Defined	1	0	0	Not Defined
Not Defined	1	0	1	Not Defined
Not Defined	1	1	0	Not Defined
Not Defined	1	1	1	Not Defined

Others are no define and invalid

"-" Don't care

Restriction: There is one dummy parameter when using Parallel interface.

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000-0000
S/W Reset	0000-0000
H/W Reset	0000-0000

- RDDSM (0Eh): Read Display Signal Mode

0EH	RDDSM (Read Display Signal Status)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)
1st parameter	1	1	↑	-	TEON	TEM	HS	VS	PixelClk	DataEn	0	ErrorDSI	(00h)-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
TEON	Tearing effect line on/off	'1' = ON, '0' = OFF,
TEM	Tearing effect line mode	'1' = mode2, '0' = mode1,
HS	Horizontal Sync (RGB interface)	'1' = ON, '0' = OFF,
VS	Vertical Sync (RGB interface)	'1' = ON, '0' = OFF,
PixelClk	Pixel Clock (DOTCLK, RGB interface)	'1' = ON, '0' = OFF,
DataEn	Data Enable (DE, RGB interface)	'1' = ON, '0' = OFF,
ErrorDSI	Error On DSI (MIPI Interface)	'1' = Error, '0' = No Error

"-" Don't care

Restriction: There is one dummy parameter when using Parallel interface.

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000-0000
S/W Reset	0000-0000
H/W Reset	0000-0000

- RDDSDR (0Fh): Read Display Self-Diagnostic Result

0FH	RDDSDR (Read Display Self-Diagnostic Result)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)
1st parameter	1	1	↑	-	RELD	FUND	-	-	-	-	-	CSCMP	(00h)
Description	This command indicates the current status of the display self-diagnostic result after sleep out command as described below: -CSCMP: Checksum comparison: '0' checksum the same; '1': checksum not the same. "-" Don't care												
Restriction	There is one dummy parameter when using Parallel interface.												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000-0000
S/W Reset	0000-0000
H/W Reset	0000-0000

- RDFCS (AAh): Read First Checksum

AAH	RDFCS (Read First Checksum)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID1	0	↑	1	-	1	0	1	0	1	0	1	0	(AAh)
1st parameter	1	1	↑	-	FCS.7-0								-
Description	*- This command returns the first checksum what has been calculated from User's area registers and the frame memory after the write access to those registers and/or frame memory has been done.* *X = can be '0' or '1'*												
Restriction	*It will be necessary to wait 150ms after there is the last write access on User area registers before there can read this checksum value.*												
Register													

availability		Status: Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default		Status: Default Value Power On Sequence: 00h S/W Reset: 00h H/W Reset: 00h

- RDCFCS (AFh): Read Continue Checksum

AFH	RDCFCS (Read Continue Checksum)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID1	0	↑	1	-	1	0	1	0	1	1	1	1	(Afh)
1st parameter	1	1	↑	-	CCS.7-0								-
Description	*- This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from User's area registers and the frame memory after the write access to those registers and/or frame memory has been done.* *X = can be '0' or '1'*												
Restriction	*It will be necessary to wait 300ms after there is the last write access on User area registers before there can read this checksum value in the first time..*												
Register availability	Status: Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes												
Default	Status: Default Value Power On Sequence: 00h H/W Reset: 00h												

- RDID1 (DAh): Read ID1

DAH	RDID1 (Read ID1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)
parameter	1	1	↑	-	ID1.7-0								-
Description	*-This read byte identifies the LCD module's manufacturer.* *'-': Don't care.*												
Register availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

- RDID2 (DBh): Read ID2

DBH	RDID2 (Read ID2)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)
1st parameter	1	1	↑	-	ID2.7-0								-
Description	*This read byte is used to track the LCD module/driver IC version.* *'-': Don't care.*												
Register availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

- RDID3 (DCh): Read ID3

DCH	RDID3 (Read ID3)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)
1st parameter	1	1	↑	-	-	ID3.7-0							-
Description	*This read byte identifies the LCD module/driver.* *'-': Don't care.*												
Register availability													
Default													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

- SLPIN (10h): Sleep in

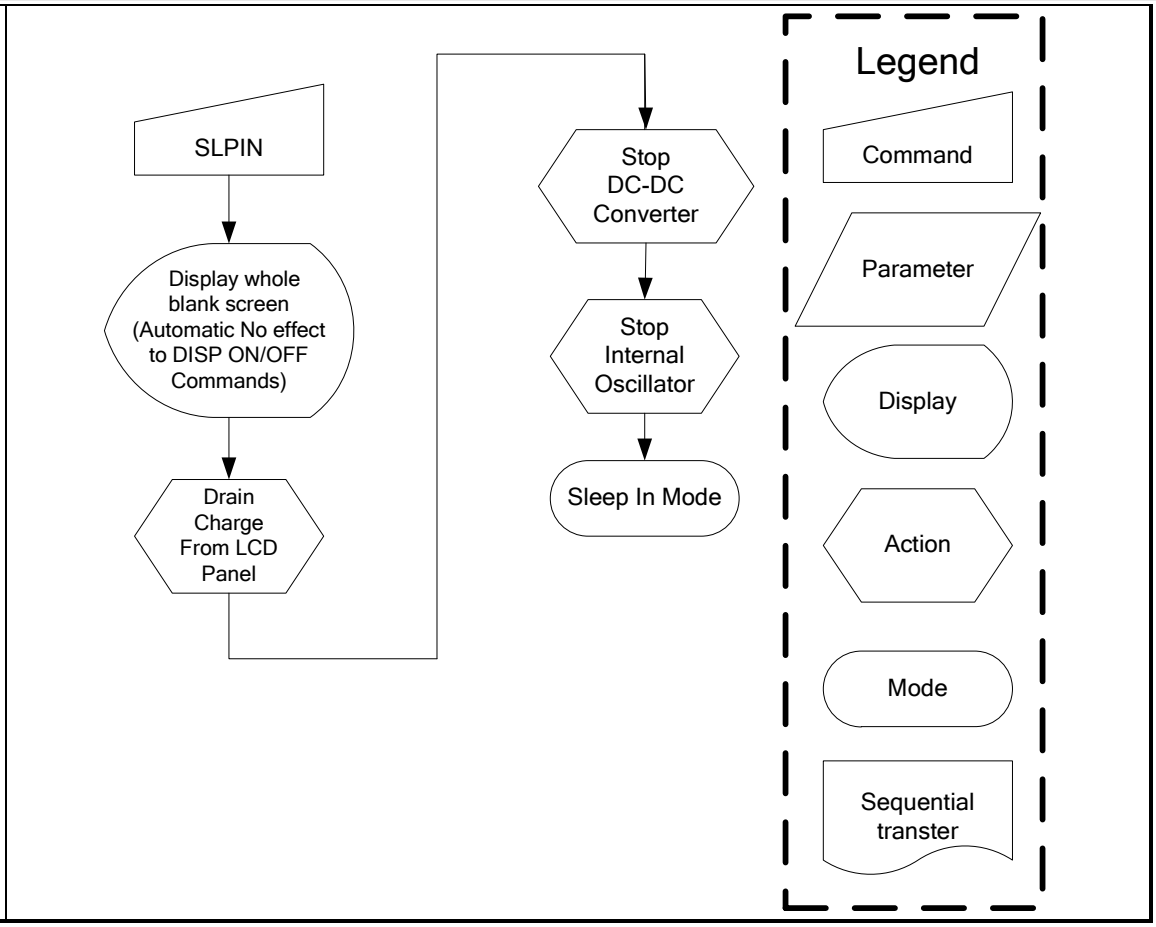
10H	SLPIN (Sleep In)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)
parameter	No Parameter												
Description	-This command causes the LCD module to enter the minimum power consumption mode. -In this mode the DC/DC converter is stopped, internal oscillator is stopped, and panel scanning is stopped. -MCU interface and memory are still working and the memory keeps its contents. -Dimming function does not work when there is changing mode from Sleep OUT to Sleep IN. "-" Don't care												
Restriction	-This command has no effect when module is already in sleep in mode. Sleep in mode can only be left by the sleep out command (11h). -It will be necessary to wait 5msec before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize. -It will be necessary to wait 120msec after sending sleep out command (when in sleep in mode) before sending an sleep in command.												
Register availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Flow Chart



- SLPOUT (11h): Sleep Out

11H	SLPOUT (Sleep Out)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)
parameter	No Parameter												
Description	-This command turn off sleep mode. -In this mode the DC/DC converter is enabled, internal display oscillator is started, and panel scanning is started.												
Restriction	-This command has no effect when module is already in sleep out mode. Sleep out mode can only be left by the sleep in command (10h). -It will be necessary to wait 5msec before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize. -It will be necessary to wait 120msec after sending sleep out command (when in sleep in mode) before sending an sleep in command. -The display module runs the self-diagnostic functions after this command is received.												
Register													

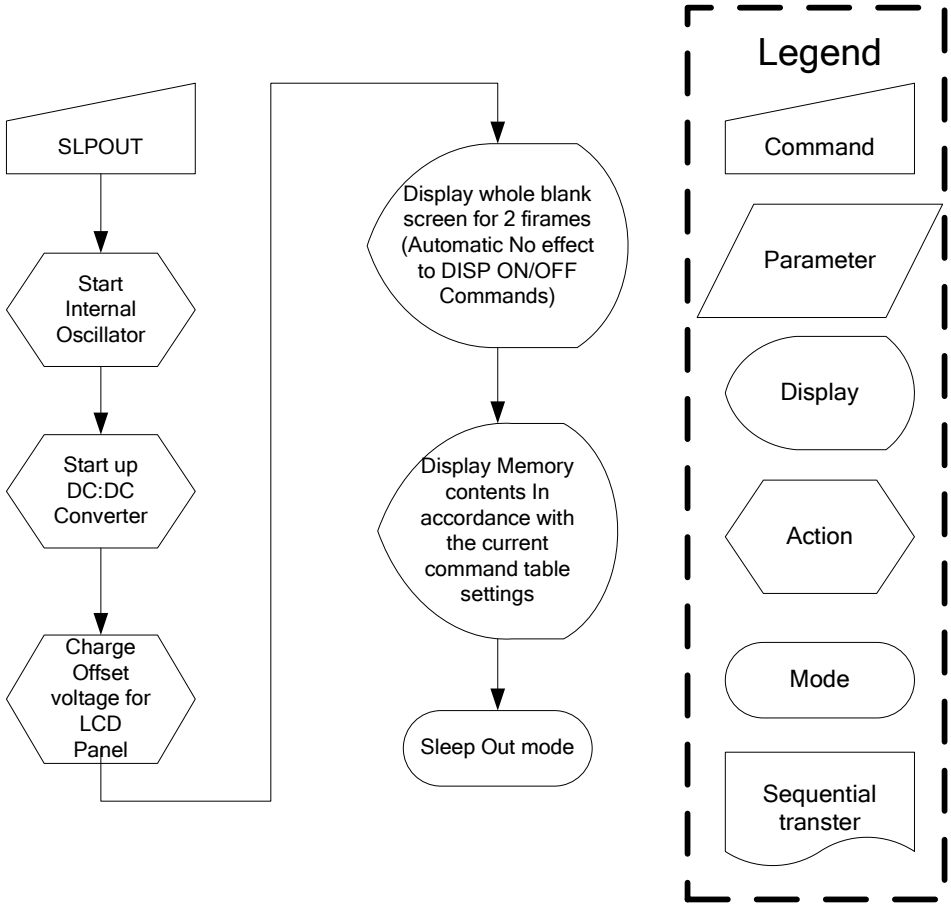
availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

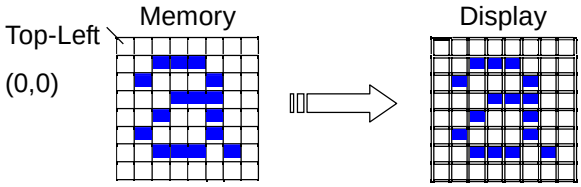
Default

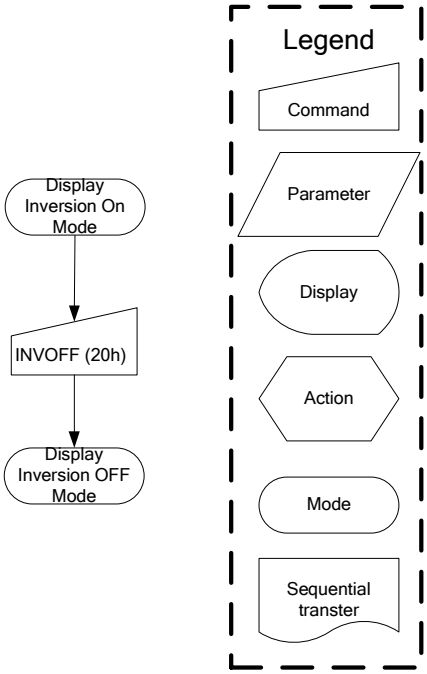
Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Flow Chart

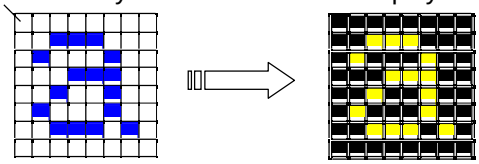


- INVOFF (20h): Display Inversion Off

<table>
<tr><td>20H</td><td colspan="13">INVOFF (Display Inversion Off)</td></tr>
<tr><td>Inst / Para</td><td>D/CX</td><td>WRX</td><td>RDX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>INVOFF</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>(20h)</td></tr>
<tr><td>parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">-This command is used to recover from display inversion mode.
“-“ Don’t care
(Example)
Top-Left (0,0) Memory Display
  </td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in inversion off mode.</td></tr>
<tr><td>Register availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display inversion off</td></tr><tr><td>S/W Reset</td><td>Display inversion off</td></tr><tr><td>H/W Reset</td><td>Display inversion off</td></tr></table></td></tr>
</table>

Flow Chart	

- INVON (21h): Display Inversion On

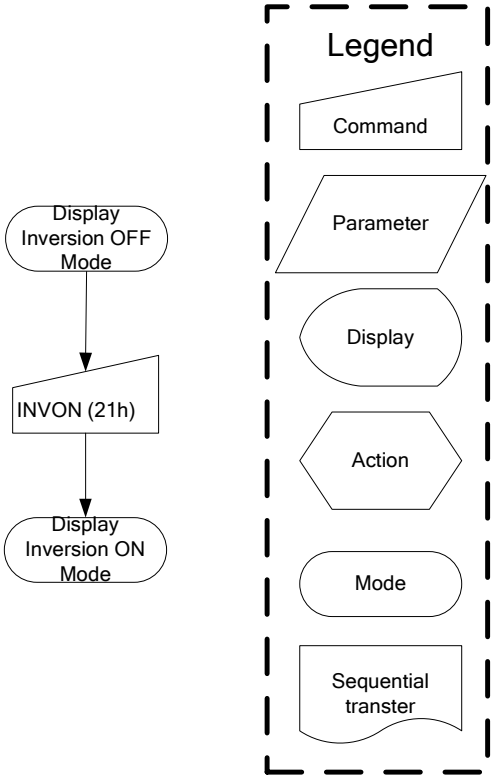
21H	INVON (Display Inversion On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)
parameter	No Parameter												
Description	*-This command is used to recover from display inversion mode.* *"-" Don't care* (Example) Top-Left (0,0) Memory Display 												
Restriction	This command has no effect when module is already in inversion on mode.												
Register availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

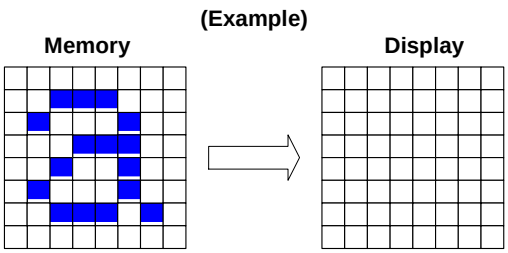
Status	Default Value
Power On Sequence	Display inversion off
S/W Reset	Display inversion off
H/W Reset	Display inversion off

Flow Chart



- DISPOFF (28h): Display Off

28H	DISPOFF (Display Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)
parameter	No Parameter												
Description	*- This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.* *- This command makes no change of contents of frame memory.* *- This command does not change any other status.* *- There will be no abnormal visible effect on the display.* *- Exit from this command by Display On (29h)*												



Restriction: This command has no effect when module is already in display off mode.

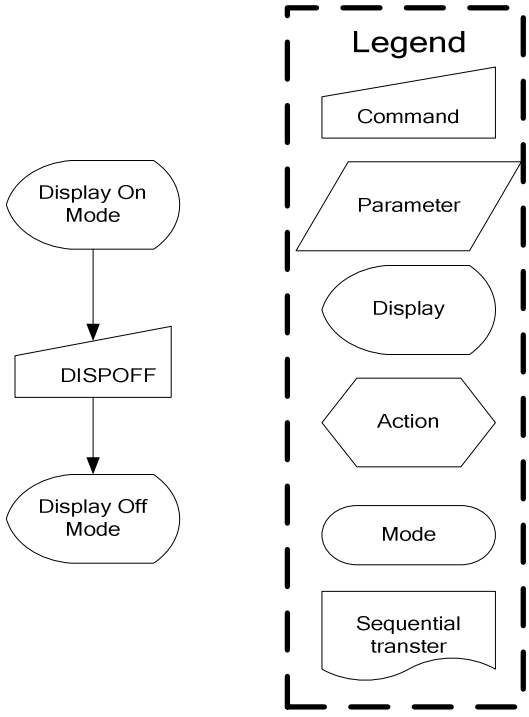
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

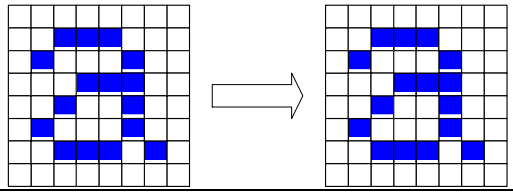
Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



- DISPON (29h): Display On

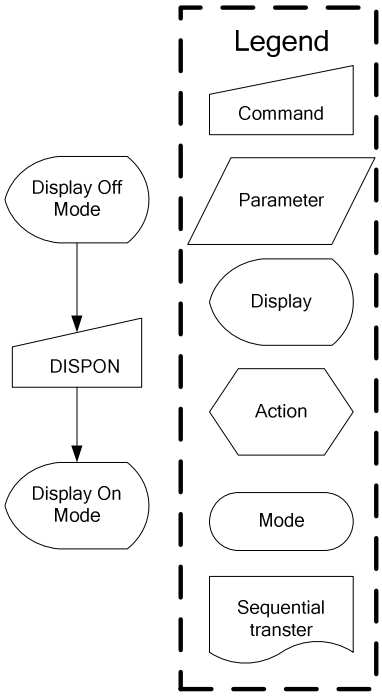
29H	DISPON (Display On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPO N	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)
parameter	No Parameter												
Description	*- This command is used to recover from DISPLAY OFF mode.* *- Output from the Frame Memory is enabled.* *- This command makes no change of contents of frame memory.* *- This command does not change any other status.* **(Example)** **Memory** **Display** 												
Restriction	This command has no effect when module is already in display on mode.												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

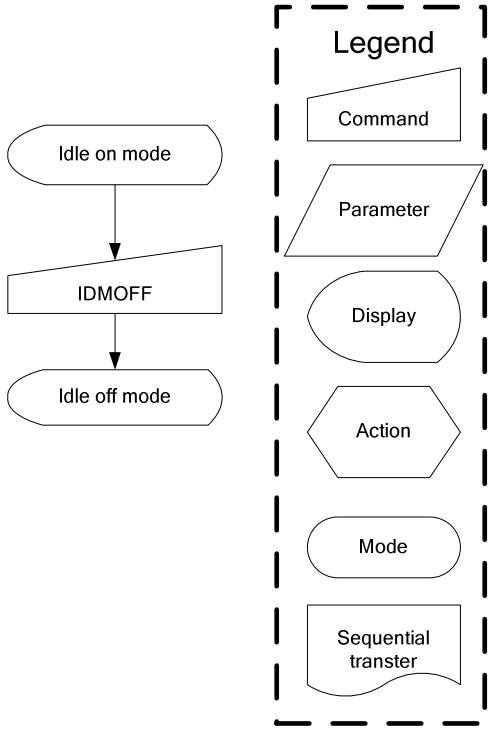
Flow Chart	

- IDMOFF (38h): Idle Mode Off

38H	IDMOFF (Idle Mode Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)
parameter	No Parameter												
Description	*-This command is used to recover from Idle mode on.* *-In the idle off mode,* *1. LCD can display 65k, 262k or 16M colors.* *2. Normal frame frequency is applied.*												
Restriction	This command has no effect when module is already in idle off mode												

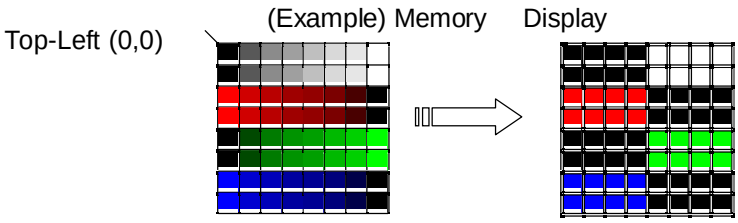
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle mode off</td></tr><tr><td>S/W Reset</td><td>Idle mode off</td></tr><tr><td>H/W Reset</td><td>Idle mode off</td></tr></table>
Flow Chart	

- IDMON (39h): Idle mode on

39H	IDMON (Idle Mode On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)
parameter	No Parameter												
Description	*-This command is used to enter into Idle mode on.* *-There will be no abnormal visible effect on the display mode change transition.* *-In the idle on mode,* *1. Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed.* *2. 8-Color mode frame frequency is applied.* *3. Exit from IDMON by Idle Mode Off (38h) command*												



Color	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B4 B1 B0
Black	0xxxxx	0xxxxx	0xxxxx
Blue	0xxxxx	0xxxxx	1xxxxx
Red	1xxxxx	0xxxxx	0xxxxx
Magenta	1xxxxx	0xxxxx	1xxxxx
Green	0xxxxx	1xxxxx	0xxxxx
Cyan	0xxxxx	1xxxxx	1xxxxx
Yellow	1xxxxx	1xxxxx	0xxxxx
White	1xxxxx	1xxxxx	1xxxxx

Restriction

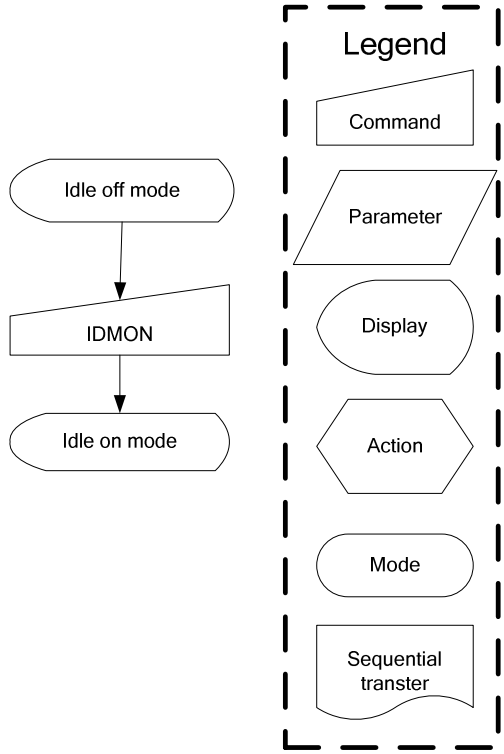
This command has no effect when module is already in idle off mode

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode off
S/W Reset	Idle mode off
H/W Reset	Idle mode off

Flow Chart	

- MADCTL (36h): Memory Data Access Control

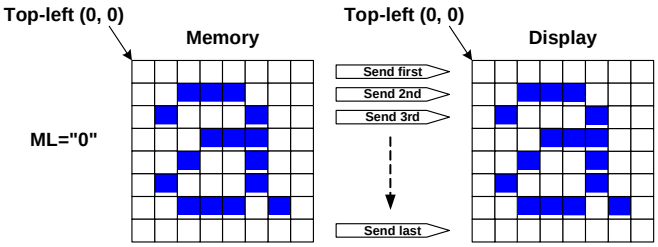
36H	MADCTL (Memory Data Access Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)
parameter	1	↑	1	-	-	-	-	ML	BGR	MH	-	-	(00h)

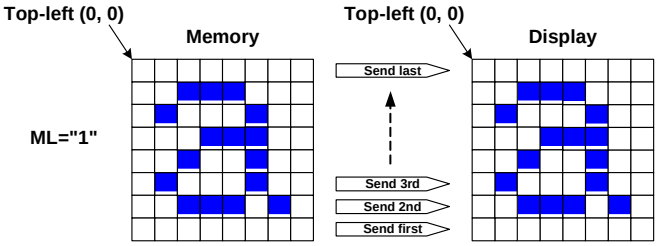
Description

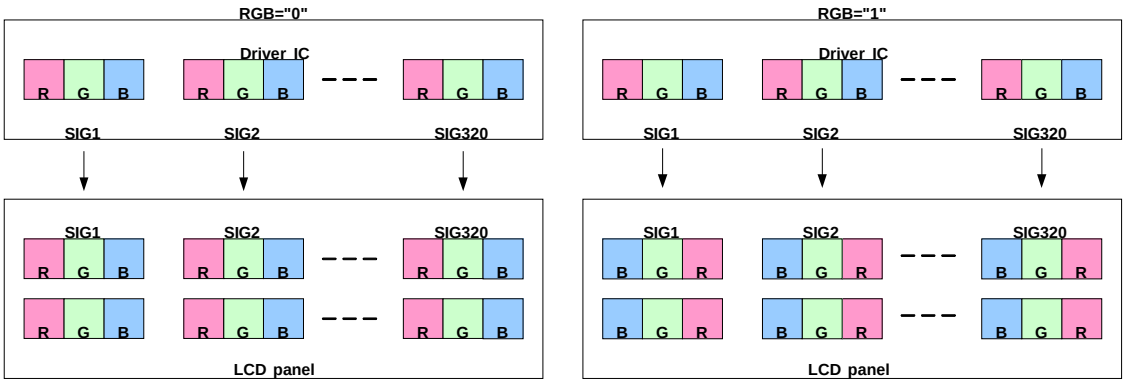
-This command defines read/ write scanning direction of frame memory.

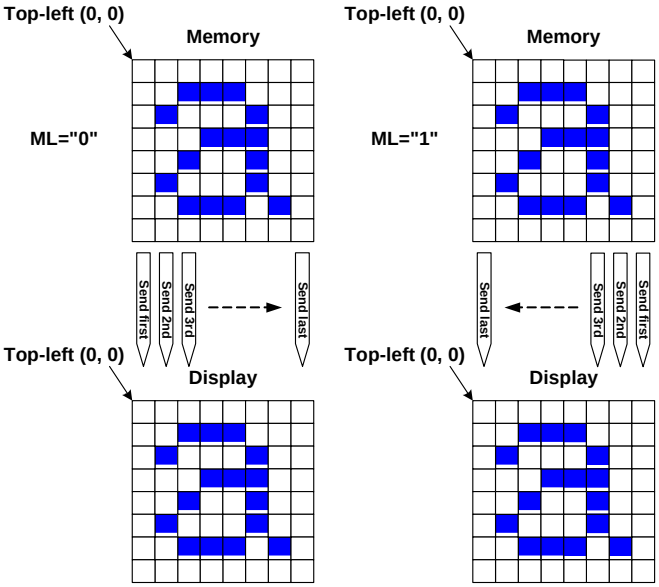
Bit	NAME	DESCRIPTION
ML	Vertical Refresh Order	LCD vertical refresh direction control '0' = LCD vertical refresh Top to Bottom '1' = LCD vertical refresh Bottom to Top
BGR	RGB-BGR ORDER	Color selector switch control '0' =RGB color filter panel, '1' =BGR color filter panel
MH	Horizontal Refresh Order	Horizontal direction '0' = Left to Right '1' = Right to Left

-Bit Assignment









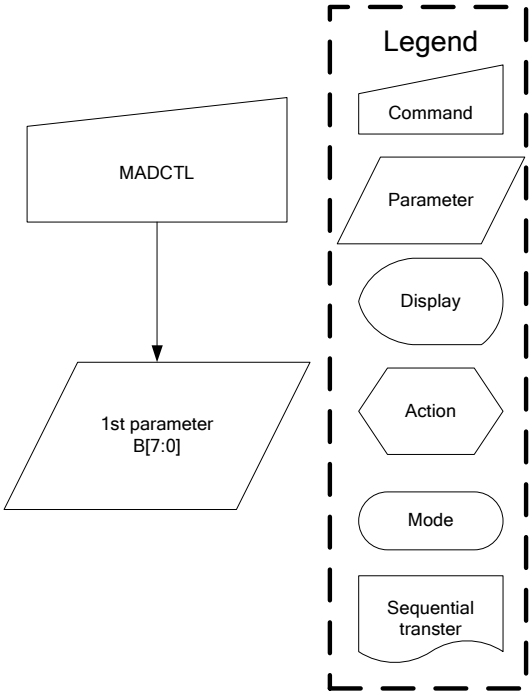
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	No change
H/W Reset	0000h

Flow Chart



- MOLMOD (3Ah): Interface Pixel Format

3AH	COLMOD (Interface Pixel Format)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)
Parameter	1	↑	1	-	-	-	-	-	-	DBI.2-0			(06h)
Description	This command is used to define the format of RGB picture data, which is to be transferred via the DBI.2-0: Display pixel input format for 1bpp mode. "101": 565 color; "110": 666 color; "111": 888 color.												

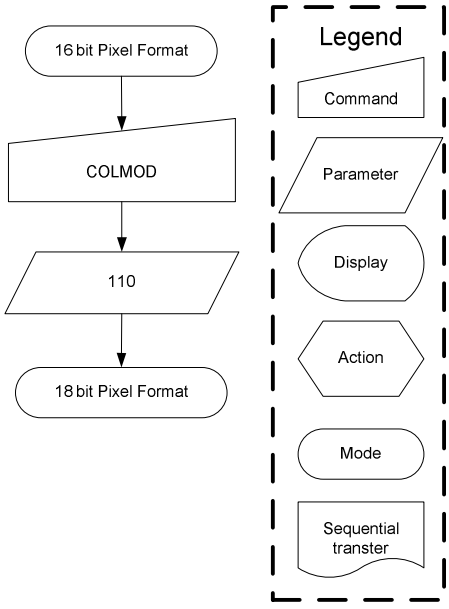
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	18bit/pixel
S/W Reset	No change
H/W Reset	18bit/pixel

Flow Chart



- RAMWR (2Ch): Memory Write

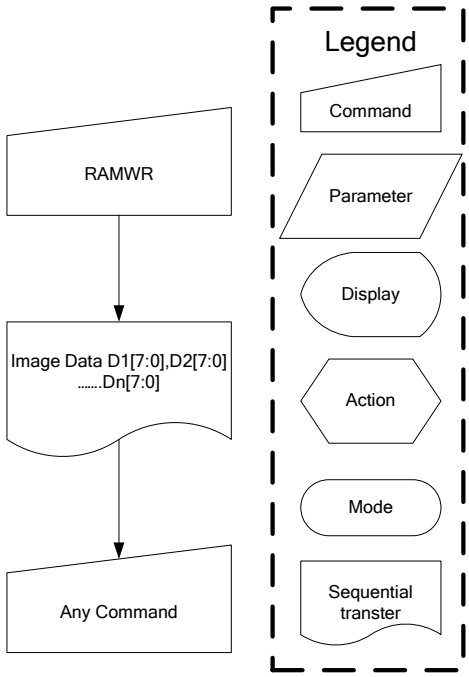
2CH	RAMWR (Memory Write)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)
1st parameter	1	↑	1	-	D1.7-0								-
…	1	↑	1	-	Dx.7-0								-
N parameter	1	↑	1	-	Dn.7-0								-
Description	*-This command is used to transfer data from MCU to frame memory.* *-When this command is accepted, the column register and the page register are reset to the start column/start page positions.* *-The start column/start page positions are different in accordance with MADCTL setting.* *-Sending any other command can stop frame write.*												
Restriction	*In all color modes, there is no restriction on length of parameters.*												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart	

- WRMEMC (3Ch): Write Memory Continue

3CH	WRMEMC (Write Memory Continue)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRMEMC	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)
1ST parameter	1	↑	1	-	D1.7-0								-
⋮	1	↑	1	-	Dx.7-0								-
Nth parameter	1	↑	1	-	Dn.7-0								-
Description	*-This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write memory continue or memory write command.:* *Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the end column (XE) value. The column register is then reset to XS and the page register is incremented. Pixels are written to the frame memory until the page register equals the end page (YE) value and the column register equals the XE value, or the host processor sends another command. If the number of pixels exceeds (XE-XS+1)*(YE-YS+1) the extra pixels are ignored.*												

Condition	Column	Page
Command 2C is accepted	Return to “Start Column”	Return to “Start Page”
Read/Write RAM action	Increment by 1	No change
Column value is large than “End Column”	Return to “Start Column”	Increment by 1
Page value is large than “End Page”	Return to “Start Column”	Return to “Start Page”

Restriction	*A memory write should follow a column address set or page address set to define the write address. Otherwise, data written with write memory continue is written to undefined addresses.*

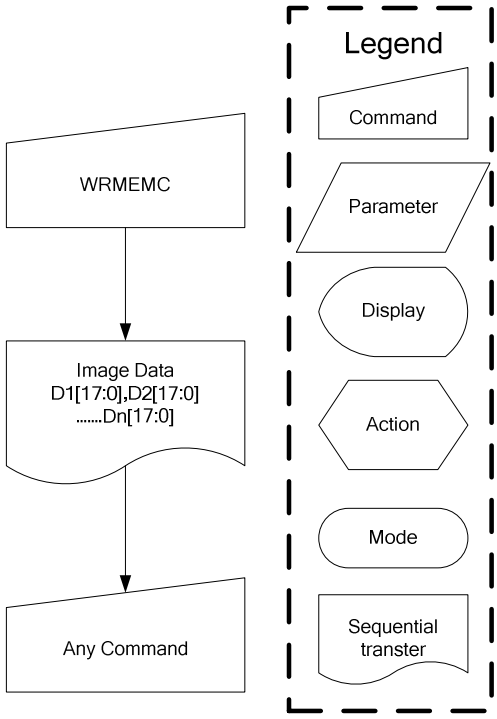
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



- TEOFF (34h): Tearing Effect Line OFF

34H	TEOFF (Tearing Effect Line OFF)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)
parameter	No Parameter												
Description	*-This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.*												
Restriction	This command has no effect when tearing effect output is already off..												

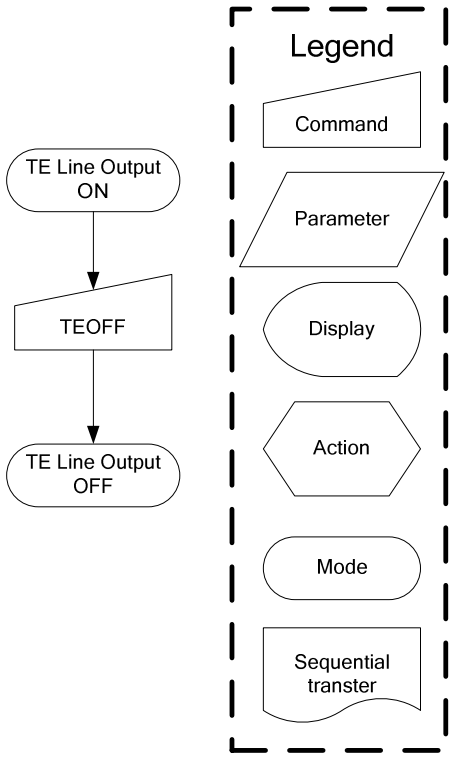
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

Flow Chart



- TEON (35h): Tearing Effect Line On

35H	TEON (Tearing Effect Line On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)
parameter	1	↑	1	-	0	0	0	0	0	0	0	TEM	

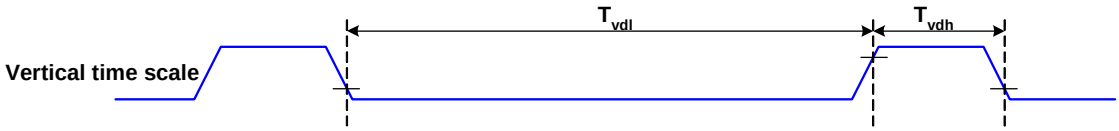
Description

-This command is used to turn ON the Tearing Effect output signal from the TE signal line.

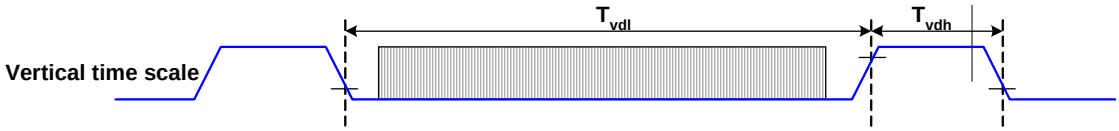
-This output is not affected by changing MADCTL bit ML.

-The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line:

-When TEM ='0': The Tearing Effect output line consists of V-Blanking information only



-When TEM ='1': The Tearing Effect output Line consists of both V-Blanking and H-Blanking information



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

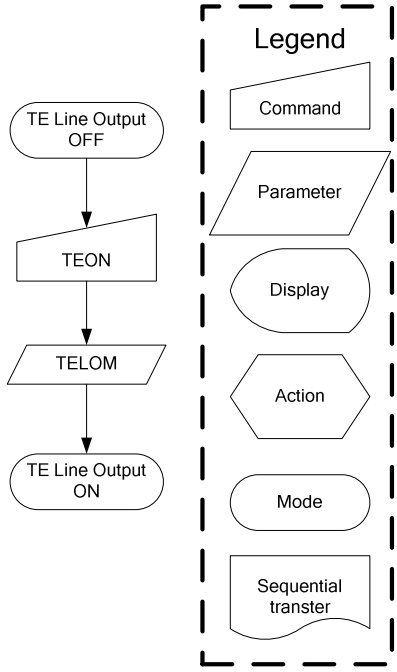
This command has no effect when tearing effect output is already on.

Register availability

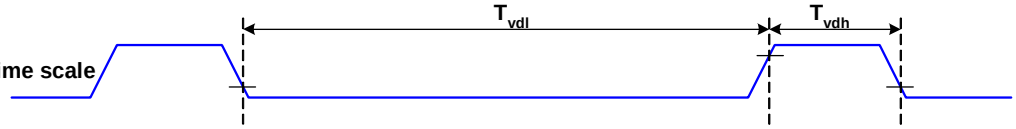
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

Flow Chart	

- STE (44h): Write Tear Scanline

44H	STE (Write Tear ScanLine)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
STE	0	↑	1	-	0	1	0	0	0	1	0	0	(44h)
1st parameter	1	↑	1	-	-	-	-	-	-	-	-	N.8	(00h)
2nd parameter	1	↑	1	-	N.7-0								(00h)
Description	*-This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The TE signal is not affected by changing MV.* *-The tearing effect line on has one parameter that describes the tearing effect output line mode.* *-The tearing effect output line consist of V-blanking information only.* **Vertical time scale**  *Note that set tear scanline with N=0 is equivalent to tearing effect line on with TEM=0.* *The tearing effect output line shall be active low when the display module is in sleep mode*												
Restriction	*This command takes affect on the frame following the current frame. Therefore, if the tear effect (TE) output is already on, the TE output shall continue to operate as programmed by the previous tearing effect line on or set tear scanline command until the end of the frame*												
Register													

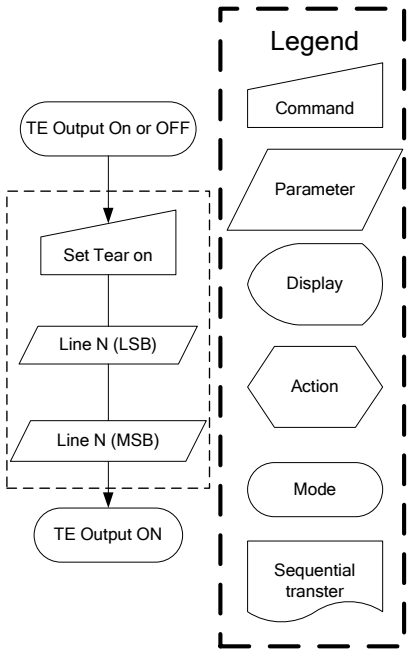
availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart



- TESLRD (45h): Read Scanline

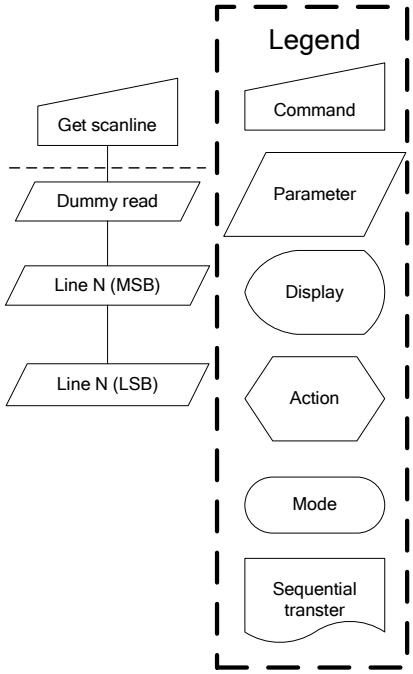
45H	TESLRD (Read ScanLine)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GSCAN	0	↑	1	-	0	1	0	0	0	1	0	1	(45h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	N.8	(00h)
2nd parameter	1	1	↑	-	N.7-0								(00h)
Description	*-The display module returns the current scanline ,N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC+VBP+VACT+VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0.* *-When in sleep in mode, the value returned by get scanline is undefined.* *Note: that Set Tear Scan Line with N = 0 is equivalent to Tearing Effect Line ON with M = 0.*												
Restriction	-												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart	

- WRIDMC (90h): Write two-color idle Mode color

90H	WRIDMC (Write two –color idle Mode color)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRIDMC	0	↑	1	-	1	0	0	1	0	0	0	0	(90h)
1st parameter	1	↑	1	-	-	-	-	-	-	R	G	B	(07h)
Description	*-The primary color of "Normal Black" panel is black, the secondary color is defined by "Write Idle Mode Color" (90h) command*												

1bpp idle mode color selection	R	G	B
Black	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Magenta	1	0	1
Yellow	1	1	0
White	1	1	1

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes

		Partial Mode On, Idle Mode On, Sleep Out	Yes
		Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

- RDIDMC (91h): Read two-color idle Mode color

91H	RDIDMC (Read two –color idle Mode color)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDIDMC	0	↑	1	-	1	0	0	1	0	0	0	1	(91h)
1st parameter	1	1	↑	-	-	-	-	-	-	R	G	B	(07h)

Description

This command indicates the tweo color current status of the display as described in the table below:

1bpp idle mode color selection	R	G	B
Black	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Magenta	1	0	1
Yellow	1	1	0
White	1	1	1

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

13.3. Cmmand Table 2

- ECFC (B0h): Entry Code Function Control

B0H	Entry Code Function Control												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
ECFC	0	↑	1	-	1	0	1	1	0	0	0	0	(B0h)
parameter	1	↑	1	-	EC.7-0								(02h)-
Description	*-Entry code to initiate specific operation*												

EC.7-0	Operation
0xA5	Enable test image generation (Reading of CmdoxBo.Po[0] = PG_GO = 1)
0x5A	Disable test image generation (Reading of CmdoxBo.Po[0] = PG_GO = 0) (Default)
0xC3	Enable use of 8-color idle mode (Reading of CmdoxBo.Po[1] = TCS = 0)
0x3C	Enable use of 2-color idle mode (Reading of CmdoxBo.Po[1] = TCS = 1) (Default)

'-': Don't care.

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	02h
S/W Reset	02h
H/W Reset	02h

- FRC1 (B1h): Frame Rate Control 1

B1H	Frame Rate Control 1												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FRC1	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)
1st parameter	1	↑	1	-	FRS.7-0								(FAh)
2nd parameter	1	↑	1	-	RTN.7-0								(C6h)
Description	*-FRS.7-0: frame rate coarse tune for idle mode.* *-RTN.7-0: frame rate fine tune for idle mode, 1 idle mode line period = 168 + RTN.7-0 + 256 x ((255 - FRS.7-0) (cycles)* '-': Don't care.												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	FAh/C6h
S/W Reset	FAh/C6h
H/W Reset	FAh/C6h

- GSC (B2h): Gate Scan Control

B2H	Gate Scan Control												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GSC	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)
parameter	1	↑	1	-	-	-	-	FGS	ML_GS_REV	GS.2-0			(10h)

Description

-GS.2-0: Odd/Even gate drive order.

GS.1-0	Gate drive order
3'b000	z-drive (odd,even,odd,even) for every frame
3'b001	reversed z-drive (even,odd,even,odd) for every frame
3'b010	bow-drive (odd,even,even,odd) for every frame
3'b011	reversed bow-drive (even,odd,odd,even) for every frame
3'b10x	z and reversed z-drive alternately by frame
3'b11x	bow and reversed bow-drive alternately by frame

-ML_GS_REV: Invert GS[0] (ex., Z to rev-Z) if ML=1.

	-GAT_TOG_REV: 1: to reverse gate drive right/left side order, 0: not reversed. '-': Don't care.
Register availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	10h
S/W Reset	10h
H/W Reset	10h

- VDMDC (B3h): Video Mode Display Control

B3H	Video Mode Display Control												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VDMDC	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)
parameter	1	↑	1	-	-	-	-	-	DINV_A.3-0				(01h)

Description

-DINV.1-0: Panel inversion mode setting for video mode.

DINV.3-0	Mode
0000	column inversion
0001	1-dot inversion
0010	2-dot inversion
0011	3-dot inversion
	:
1111	15-dot inversion

'-': Don't care.

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value

		Power On Sequence	01h	
		S/W Reset	01h	
		H/W Reset	01h	

- TCMDC (B4h): Two color Mode Display Control

B4H	Two color Mode Display Control												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TCMDC	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)
parameter	1	↑	1	-	-	-	-	-	DINV_B.3-0				(01h)

Description

-DINV.1-0: Panel inversion mode setting for Two color mode.

DINV.3-0	Mode
0000	column inversion
0001	1-dot inversion
0010	2-dot inversion
0011	3-dot inversion
	:
1111	15-dot inversion

'-': Don't care.

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

● BPC (B5h): Blank Porch Control

B5H	Blank Porch Control												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
BPC	0	↑	1	-	1	0	1	1	0	1	0	1	(B5h)
1st parameter	1	↑	1	-	VFP.15-8								(00h)
2nd parameter	1	↑	1	-	VFP.7-0								(02h)
3rd parameter	1	↑	1	-	VBP.15-8								(00h)
4th parameter	1	↑	1	-	VBP.7-0								(03h)
Description	-VFP.15-0: The number of lines in vertical front porch period for idle mode. -VBP.15-0: The number of lines in vertical back porch period for idle mode. Note that valid range of VFP and VBP are between 2 and 65535. When in idle mode, hardware uses VFP.15-0 and VBP.15-0 for porch control. "-" Don't care												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

● EMSET (B7h): Entry Mode Set

B7H	Entry Mode Set												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
BPC	0	↑	1	-	1	0	1	1	0	1	1	1	(B7h)
parameter	1	↑	1	-	-	-	-	-	DSTB	-	-	-	(00h)
Description	*-DSTB: Deep standby mode. '1' for going to deep standby mode. In this mode,* *logic power and SRAM power are turned off.* *-exit the standby mode: by pull down RESX.* "-" Don't care												

Register availability		Status	Availability
		Normal Mode On, Idle Mode Off, Sleep Out	Yes
		Normal Mode On, Idle Mode On, Sleep Out	Yes
		Partial Mode On, Idle Mode Off, Sleep Out	Yes
		Partial Mode On, Idle Mode On, Sleep Out	Yes
		Sleep In	Yes
Default		Status	Default Value
		Power On Sequence	00h
		S/W Reset	00h
		H/W Reset	00h

- PWR1 (C1h): Power Control 1

C1H	Power Control 1												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWR1	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)
1st parameter	1	↑	1	-	VGHS2_A.3-0				VGHS1_A.3-0				(44h)
2nd parameter	1	↑	1	-	-	-	-	-	VGLS_A.3-0				(06h)
3rd parameter	1	↑	1	-	VPMS_A.3-0				VNMS_A.3-0				(ACh)
4th parameter	1	↑	1	-	-	-	VRH_A.5-0						(1Bh)

Description

-C1h Function for Video mode

-VGHS1.3-0: STEP2 VGH voltage level selection.

-VGHS2.3-0: STEP2S VGHS voltage level selection.

-VGLS.3-0: STEP3 VGL voltage level selection.

No.	VGHS1.3-0 VGHS2.3-0	VGH (V) VGHS(V)	VGLS.3-0	VGL (V)
0	0000	12.541	0000	-8.210
1	0001	12.889	0001	-8.484
2	0010	13.257	0010	-8.773
3	0011	13.647	0011	-9.078
4	0100	14.061	0100	-9.400
5	0101	14.500	0101	-9.741
6	0110	14.968	0110	-10.103
7	0111	15.467	0111	-10.488
8	1000	16.000	1000	-10.897
9	1001	Reserved	1001	-11.333
10	1010		1010	-11.800
11	1011		1011	Reserved
12	1100		1100	
13	1101		1101	
14	1110		1110	
15	1111		1111	

Description

-VPMS.3-0: STEP1 AVDD voltage level selection.

-VNMS.3-0: STEP4 AVEE voltage level selection.

No.	VPMS.3-0	AVDD(V)	VNMS.3-0	AVEE(V)
0	0000	5.691	0000	-3.270
1	0001	5.775	0001	-3.344
2	0010	5.860	0010	-3.412
3	0011	5.947	0011	-3.486
4	0100	6.003	0100	-3.562
5	0101	6.129	0101	-3.640
6	0110	6.225	0110	-3.721
7	0111	6.323	0111	-3.804
8	1000	6.425	1000	-3.889
9	1001	6.535	1001	-3.977
10	1010	6.666	1010	-4.067
11	1011	6.756	1011	-4.161
12	1100	6.872	1100	-4.257
13	1101	6.993	1101	-4.356
14	1110	7.532	1110	-4.459
15	1111	7.678	1111	-4.563

-VRH.5-0: Gamma resistor VREGP and VREGN voltage level selection.

No.	VRHP.6-0	VREGP(V)	No.	VRHP.6-0	VREGP(V)	No.	VRHP.6-0	VREGP(V)	No.	VRHP.6-0	VREGP(V)
0	0000000	3.650	32	0100000	4.450	64	1000000	5.250	96	1100000	6.050
1	0000001	3.675	33	0100001	4.475	65	1000001	5.275	97	1100001	6.075
2	0000010	3.700	34	0100010	4.500	66	1000010	5.300	98	1100010	6.100
3	0000011	3.725	35	0100011	4.525	67	1000011	5.325	99	1100011	6.125
4	0000100	3.750	36	0100100	4.550	68	1000100	5.350	100	1100100	6.150
5	0000101	3.775	37	0100101	4.575	69	1000101	5.375	101	1100101	6.175
6	0000110	3.800	38	0100110	4.600	70	1000110	5.400	102	1100110	6.200
7	0000111	3.825	39	0100111	4.625	71	1000111	5.425	103	1100111	6.225
8	0001000	3.850	40	0101000	4.650	72	1001000	5.450	104	1101000	6.250
9	0001001	3.875	41	0101001	4.675	73	1001001	5.475	105	1101001	6.275
10	0001010	3.900	42	0101010	4.700	74	1001010	5.500	106	1101010	6.300
11	0001011	3.925	43	0101011	4.725	75	1001011	5.525	107	1101011	6.325
12	0001100	3.950	44	0101100	4.750	76	1001100	5.550	108	1101100	6.350
13	0001101	3.975	45	0101101	4.775	77	1001101	5.575	109	1101101	6.375
14	0001110	4.000	46	0101110	4.800	78	1001110	5.600	110	1101110	6.400
15	0001111	4.025	47	0101111	4.825	79	1001111	5.625	111	1101111	6.425
16	0010000	4.050	48	0110000	4.850	80	1010000	5.650	112	1110000	6.450
17	0010001	4.075	49	0110001	4.875	81	1010001	5.675	113	1110001	6.475
18	0010010	4.100	50	0110010	4.900	82	1010010	5.700	114	1110010	6.500
19	0010011	4.125	51	0110011	4.925	83	1010011	5.725	115	1110011	6.525
20	0010100	4.150	52	0110100	4.950	84	1010100	5.750	116	1110100	6.550
21	0010101	4.175	53	0110101	4.975	85	1010101	5.775	117	1110101	6.575
22	0010110	4.200	54	0110110	5.000	86	1010110	5.800	118	1110110	6.600
23	0010111	4.225	55	0110111	5.025	87	1010111	5.825	119	1110111	6.625
24	0011000	4.250	56	0111000	5.050	88	1011000	5.850	120	1111000	6.650
25	0011001	4.275	57	0111001	5.075	89	1011001	5.875	121	1111001	6.675
26	0011010	4.300	58	0111010	5.100	90	1011010	5.900	122	1111010	6.700
27	0011011	4.325	59	0111011	5.125	91	1011011	5.925	123	1111011	6.725
28	0011100	4.350	60	0111100	5.150	92	1011100	5.950	124	1111100	6.750
29	0011101	4.375	61	0111101	5.175	93	1011101	5.975	125	1111101	6.775
30	0011110	4.400	62	0111110	5.200	94	1011110	6.000	126	1111110	6.800
31	0011111	4.425	63	0111111	5.225	95	1011111	6.025	127	1111111	6.825

Description

No.	VRHN.6-0	VREGN(V)	No.	VRHN.6-0	VREGN(V)	No.	VRHN.6-0	VREGN(V)	No.	VRHN.6-0	VREGN(V)
0	0000000	-1.875	32	0100000	-2.675	64	1000000	-3.475	96	1100000	-4.275
1	0000001	-1.900	33	0100001	-2.700	65	1000001	-3.500	97	1100001	-4.300
2	0000010	-1.925	34	0100010	-2.725	66	1000010	-3.525	98	1100010	-4.325
3	0000011	-1.950	35	0100011	-2.750	67	1000011	-3.550	99	1100011	-4.350
4	0000100	-1.975	36	0100100	-2.775	68	1000100	-3.575	100	1100100	-4.375
5	0000101	-2.000	37	0100101	-2.800	69	1000101	-3.600	101	1100101	-4.400
6	0000110	-2.025	38	0100110	-2.825	70	1000110	-3.625	102	1100110	-4.425
7	0000111	-2.050	39	0100111	-2.850	71	1000111	-3.650	103	1100111	-4.450
8	0001000	-2.075	40	0101000	-2.875	72	1001000	-3.675	104	1101000	-4.475
9	0001001	-2.100	41	0101001	-2.900	73	1001001	-3.700	105	1101001	-4.500
10	0001010	-2.125	42	0101010	-2.925	74	1001010	-3.725	106	1101010	-4.525
11	0001011	-2.150	43	0101011	-2.950	75	1001011	-3.750	107	1101011	-4.550
12	0001100	-2.175	44	0101100	-2.975	76	1001100	-3.775	108	1101100	-4.575
13	0001101	-2.200	45	0101101	-3.000	77	1001101	-3.800	109	1101101	-4.600
14	0001110	-2.225	46	0101110	-3.025	78	1001110	-3.825	110	1101110	-4.625
15	0001111	-2.250	47	0101111	-3.050	79	1001111	-3.850	111	1101111	-4.650
16	0010000	-2.275	48	0110000	-3.075	80	1010000	-3.875	112	1110000	-4.675
17	0010001	-2.300	49	0110001	-3.100	81	1010001	-3.900	113	1110001	-4.700
18	0010010	-2.325	50	0110010	-3.125	82	1010010	-3.925	114	1110010	-4.725
19	0010011	-2.350	51	0110011	-3.150	83	1010011	-3.950	115	1110011	-4.750
20	0010100	-2.375	52	0110100	-3.175	84	1010100	-3.975	116	1110100	-4.775
21	0010101	-2.400	53	0110101	-3.200	85	1010101	-4.000	117	1110101	-4.800
22	0010110	-2.425	54	0110110	-3.225	86	1010110	-4.025	118	1110110	-4.825
23	0010111	-2.450	55	0110111	-3.250	87	1010111	-4.050	119	1110111	-4.850
24	0011000	-2.475	56	0111000	-3.275	88	1011000	-4.075	120	1111000	-4.875
25	0011001	-2.500	57	0111001	-3.300	89	1011001	-4.100	121	1111001	-4.900
26	0011010	-2.525	58	0111010	-3.325	90	1011010	-4.125	122	1111010	-4.925
27	0011011	-2.550	59	0111011	-3.350	91	1011011	-4.150	123	1111011	-4.950
28	0011100	-2.575	60	0111100	-3.375	92	1011100	-4.175	124	1111100	-4.975
29	0011101	-2.600	61	0111101	-3.400	93	1011101	-4.200	125	1111101	-5.000
30	0011110	-2.625	62	0111110	-3.425	94	1011110	-4.225	126	1111110	-5.025
31	0011111	-2.650	63	0111111	-3.450	95	1011111	-4.250	127	1111111	-5.050

"-" Don't care

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

- PWR2 (C2h): Power Control 2

C2H	Power Control 2												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWR2	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)
1st parameter	1	↑	1	-	VGHS2_B.3-0				VGHS1_B.3-0				(44h)
2nd parameter	1	↑	1	-	-	-	-	-	VGLS_B.3-0				(06h)
3rd parameter	1	↑	1	-	VPMS_B.3-0				VNMS_B.3-0				(ACh)
4th parameter	1	↑	1	-	-	-	VRH_B.5-0						(1Bh)

Description

-C2h Function for Idle mode

-VGHS1.3-0: STEP2 VGH voltage level selection.

-VGHS2.3-0: STEP2S VGHS voltage level selection.

-VGLS.3-0: STEP3 VGL voltage level selection.

No.	VGHS1.3-0 VGHS2.3-0	VGH (V) VGHS(V)	VGLS.3-0	VGL (V)
0	0000	12.541	0000	-8.210
1	0001	12.889	0001	-8.484
2	0010	13.257	0010	-8.773
3	0011	13.647	0011	-9.078
4	0100	14.061	0100	-9.400
5	0101	14.500	0101	-9.741
6	0110	14.968	0110	-10.103
7	0111	15.467	0111	-10.488
8	1000	16.000	1000	-10.897
9	1001	Reserved	1001	-11.333
10	1010		1010	-11.800
11	1011		1011	Reserved
12	1100		1100	
13	1101		1101	
14	1110		1110	
15	1111		1111	

Description

-VPMS.3-0: STEP1 AVDD voltage level selection.

-VNMS.3-0: STEP4 AVEE voltage level selection.

No.	VPMS.3-0	AVDD(V)	VNMS.3-0	AVEE(V)
0	0000	5.691	0000	-3.270
1	0001	5.775	0001	-3.344
2	0010	5.860	0010	-3.412
3	0011	5.947	0011	-3.486
4	0100	6.003	0100	-3.562
5	0101	6.129	0101	-3.640
6	0110	6.225	0110	-3.721
7	0111	6.323	0111	-3.804
8	1000	6.425	1000	-3.889
9	1001	6.535	1001	-3.977
10	1010	6.666	1010	-4.067
11	1011	6.756	1011	-4.161
12	1100	6.872	1100	-4.257
13	1101	6.993	1101	-4.356
14	1110	7.532	1110	-4.459
15	1111	7.678	1111	-4.563

-VRH.5-0: Gamma resistor VREGP and VREGN voltage level selection.

No.	VRHP.6-0	VREGP(V)	No.	VRHP.6-0	VREGP(V)	No.	VRHP.6-0	VREGP(V)	No.	VRHP.6-0	VREGP(V)
0	0000000	3.650	32	0100000	4.450	64	1000000	5.250	96	1100000	6.050
1	0000001	3.675	33	0100001	4.475	65	1000001	5.275	97	1100001	6.075
2	0000010	3.700	34	0100010	4.500	66	1000010	5.300	98	1100010	6.100
3	0000011	3.725	35	0100011	4.525	67	1000011	5.325	99	1100011	6.125
4	0000100	3.750	36	0100100	4.550	68	1000100	5.350	100	1100100	6.150
5	0000101	3.775	37	0100101	4.575	69	1000101	5.375	101	1100101	6.175
6	0000110	3.800	38	0100110	4.600	70	1000110	5.400	102	1100110	6.200
7	0000111	3.825	39	0100111	4.625	71	1000111	5.425	103	1100111	6.225
8	0001000	3.850	40	0101000	4.650	72	1001000	5.450	104	1101000	6.250
9	0001001	3.875	41	0101001	4.675	73	1001001	5.475	105	1101001	6.275
10	0001010	3.900	42	0101010	4.700	74	1001010	5.500	106	1101010	6.300
11	0001011	3.925	43	0101011	4.725	75	1001011	5.525	107	1101011	6.325
12	0001100	3.950	44	0101100	4.750	76	1001100	5.550	108	1101100	6.350
13	0001101	3.975	45	0101101	4.775	77	1001101	5.575	109	1101101	6.375
14	0001110	4.000	46	0101110	4.800	78	1001110	5.600	110	1101110	6.400
15	0001111	4.025	47	0101111	4.825	79	1001111	5.625	111	1101111	6.425
16	0010000	4.050	48	0110000	4.850	80	1010000	5.650	112	1110000	6.450
17	0010001	4.075	49	0110001	4.875	81	1010001	5.675	113	1110001	6.475
18	0010010	4.100	50	0110010	4.900	82	1010010	5.700	114	1110010	6.500
19	0010011	4.125	51	0110011	4.925	83	1010011	5.725	115	1110011	6.525
20	0010100	4.150	52	0110100	4.950	84	1010100	5.750	116	1110100	6.550
21	0010101	4.175	53	0110101	4.975	85	1010101	5.775	117	1110101	6.575
22	0010110	4.200	54	0110110	5.000	86	1010110	5.800	118	1110110	6.600
23	0010111	4.225	55	0110111	5.025	87	1010111	5.825	119	1110111	6.625
24	0011000	4.250	56	0111000	5.050	88	1011000	5.850	120	1111000	6.650
25	0011001	4.275	57	0111001	5.075	89	1011001	5.875	121	1111001	6.675
26	0011010	4.300	58	0111010	5.100	90	1011010	5.900	122	1111010	6.700
27	0011011	4.325	59	0111011	5.125	91	1011011	5.925	123	1111011	6.725
28	0011100	4.350	60	0111100	5.150	92	1011100	5.950	124	1111100	6.750
29	0011101	4.375	61	0111101	5.175	93	1011101	5.975	125	1111101	6.775
30	0011110	4.400	62	0111110	5.200	94	1011110	6.000	126	1111110	6.800
31	0011111	4.425	63	0111111	5.225	95	1011111	6.025	127	1111111	6.825

Description

No.	VRHN.6-0	VREGN(V)	No.	VRHN.6-0	VREGN(V)	No.	VRHN.6-0	VREGN(V)	No.	VRHN.6-0	VREGN(V)
0	0000000	-1.875	32	0100000	-2.675	64	1000000	-3.475	96	1100000	-4.275
1	0000001	-1.900	33	0100001	-2.700	65	1000001	-3.500	97	1100001	-4.300
2	0000010	-1.925	34	0100010	-2.725	66	1000010	-3.525	98	1100010	-4.325
3	0000011	-1.950	35	0100011	-2.750	67	1000011	-3.550	99	1100011	-4.350
4	0000100	-1.975	36	0100100	-2.775	68	1000100	-3.575	100	1100100	-4.375
5	0000101	-2.000	37	0100101	-2.800	69	1000101	-3.600	101	1100101	-4.400
6	0000110	-2.025	38	0100110	-2.825	70	1000110	-3.625	102	1100110	-4.425
7	0000111	-2.050	39	0100111	-2.850	71	1000111	-3.650	103	1100111	-4.450
8	0001000	-2.075	40	0101000	-2.875	72	1001000	-3.675	104	1101000	-4.475
9	0001001	-2.100	41	0101001	-2.900	73	1001001	-3.700	105	1101001	-4.500
10	0001010	-2.125	42	0101010	-2.925	74	1001010	-3.725	106	1101010	-4.525
11	0001011	-2.150	43	0101011	-2.950	75	1001011	-3.750	107	1101011	-4.550
12	0001100	-2.175	44	0101100	-2.975	76	1001100	-3.775	108	1101100	-4.575
13	0001101	-2.200	45	0101101	-3.000	77	1001101	-3.800	109	1101101	-4.600
14	0001110	-2.225	46	0101110	-3.025	78	1001110	-3.825	110	1101110	-4.625
15	0001111	-2.250	47	0101111	-3.050	79	1001111	-3.850	111	1101111	-4.650
16	0010000	-2.275	48	0110000	-3.075	80	1010000	-3.875	112	1110000	-4.675
17	0010001	-2.300	49	0110001	-3.100	81	1010001	-3.900	113	1110001	-4.700
18	0010010	-2.325	50	0110010	-3.125	82	1010010	-3.925	114	1110010	-4.725
19	0010011	-2.350	51	0110011	-3.150	83	1010011	-3.950	115	1110011	-4.750
20	0010100	-2.375	52	0110100	-3.175	84	1010100	-3.975	116	1110100	-4.775
21	0010101	-2.400	53	0110101	-3.200	85	1010101	-4.000	117	1110101	-4.800
22	0010110	-2.425	54	0110110	-3.225	86	1010110	-4.025	118	1110110	-4.825
23	0010111	-2.450	55	0110111	-3.250	87	1010111	-4.050	119	1110111	-4.850
24	0011000	-2.475	56	0111000	-3.275	88	1011000	-4.075	120	1111000	-4.875
25	0011001	-2.500	57	0111001	-3.300	89	1011001	-4.100	121	1111001	-4.900
26	0011010	-2.525	58	0111010	-3.325	90	1011010	-4.125	122	1111010	-4.925
27	0011011	-2.550	59	0111011	-3.350	91	1011011	-4.150	123	1111011	-4.950
28	0011100	-2.575	60	0111100	-3.375	92	1011100	-4.175	124	1111100	-4.975
29	0011101	-2.600	61	0111101	-3.400	93	1011101	-4.200	125	1111101	-5.000
30	0011110	-2.625	62	0111110	-3.425	94	1011110	-4.225	126	1111110	-5.025
31	0011111	-2.650	63	0111111	-3.450	95	1011111	-4.250	127	1111111	-5.050

"-" Don't care

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

- VCOMCTL (C5h): Vcom Control

C5H	Vcom Control												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VCOMCTL	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)
parameter	1	↑	1	-	VMF_MODE	VCOM.6-0							(57h)

Description

-VCOM.6-0: To control gamma VSF voltage level selection.

VMF_MODE	Description
0	VMF1.6-0/VMF2.6-0 will be valued copied from OTP.
1	VMF1.6-0/VMF2.6-0 will be valued provided by users.

No.	VCM[6:0]	VSF (V)	No.	VCM[6:0]	VSF (V)	No.	VCM[6:0]	VSF (V)	No.	VCM[6:0]	VSF (V)
0	0000000	0.000	32	0100000	0.000	64	1000000	0.625	96	1100000	1.425
1	0000001	0.000	33	0100001	0.000	65	1000001	0.650	97	1100001	1.450
2	0000010	0.000	34	0100010	0.000	66	1000010	0.675	98	1100010	1.475
3	0000011	0.000	35	0100011	0.000	67	1000011	0.700	99	1100011	1.500
4	0000100	0.000	36	0100100	0.000	68	1000100	0.725	100	1100100	1.525
5	0000101	0.000	37	0100101	0.000	69	1000101	0.750	101	1100101	1.550
6	0000110	0.000	38	0100110	0.000	70	1000110	0.775	102	1100110	1.575
7	0000111	0.000	39	0100111	0.000	71	1000111	0.800	103	1100111	1.600
8	0001000	0.000	40	0101000	0.025	72	1001000	0.825	104	1101000	1.625
9	0001001	0.000	41	0101001	0.050	73	1001001	0.850	105	1101001	1.650
10	0001010	0.000	42	0101010	0.075	74	1001010	0.875	106	1101010	1.675
11	0001011	0.000	43	0101011	0.100	75	1001011	0.900	107	1101011	1.700
12	0001100	0.000	44	0101100	0.125	76	1001100	0.925	108	1101100	1.725
13	0001101	0.000	45	0101101	0.150	77	1001101	0.950	109	1101101	1.750
14	0001110	0.000	46	0101110	0.175	78	1001110	0.975	110	1101110	1.775
15	0001111	0.000	47	0101111	0.200	79	1001111	1.000	111	1101111	1.800
16	0010000	0.000	48	0110000	0.225	80	1010000	1.025	112	1110000	1.825
17	0010001	0.000	49	0110001	0.250	81	1010001	1.050	113	1110001	1.850
18	0010010	0.000	50	0110010	0.275	82	1010010	1.075	114	1110010	1.875
19	0010011	0.000	51	0110011	0.300	83	1010011	1.100	115	1110011	1.900
20	0010100	0.000	52	0110100	0.325	84	1010100	1.125	116	1110100	1.925
21	0010101	0.000	53	0110101	0.350	85	1010101	1.150	117	1110101	1.950
22	0010110	0.000	54	0110110	0.375	86	1010110	1.175	118	1110110	1.975
23	0010111	0.000	55	0110111	0.400	87	1010111	1.200	119	1110111	2.000
24	0011000	0.000	56	0111000	0.425	88	1011000	1.225	120	1111000	2.025
25	0011001	0.000	57	0111001	0.450	89	1011001	1.250	121	1111001	2.050
26	0011010	0.000	58	0111010	0.475	90	1011010	1.275	122	1111010	2.075
27	0011011	0.000	59	0111011	0.500	91	1011011	1.300	123	1111011	2.100
28	0011100	0.000	60	0111100	0.525	92	1011100	1.325	124	1111100	2.125
29	0011101	0.000	61	0111101	0.550	93	1011101	1.350	125	1111101	2.150
30	0011110	0.000	62	0111110	0.575	94	1011110	1.375	126	1111110	2.175
31	0011111	0.000	63	0111111	0.600	95	1011111	1.400	127	1111111	2.200

"-" Don't care

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default		Status	Default Value
		Power On Sequence	57h
		S/W Reset	57h
		H/W Reset	57h

- PGC (E0h): Positive Gamma Control

E0H	Positive Gamma Control												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PGC	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)
1st parameter	1	↑	1	-	VC63P.3-0				VC0P.3-0				(F0h)
2nd parameter	1	↑	1	-	-	-	VC1P.5-0						(03h)
3rd parameter	1	↑	1	-	-	-	VC2P.5-0						(05h)
4th parameter	1	↑	1	-	-	-	-	VC4P.4-0					(09h)
5th parameter	1	↑	1	-	-	-	-	VC6P.4-0					(0Ch)
6th parameter	1	↑	1	-	-	VJ0P.2-0			VC13P.3-0				(0Fh)
7th parameter	1	↑	1	-	-	VC20P.6-0							(3Eh)
8th parameter	1	↑	1	-	-	VC36P.2-0			-	VC27P.2-0			(77h)
9th parameter	1	↑	1	-	-	VC43P.6-0							(4Fh)
10th parameter	1	↑	1	-	-	VJ1P.2-0			VC50P.3-0				(0Fh)
11th parameter	1	↑	1	-	-	-	-	VC57P.4-0					(17h)
12th parameter	1	↑	1	-	-	-	-	VC59P.4-0					(17h)
13th parameter	1	↑	1	-	-	-	VC61P.5-0						(21h)
14th parameter	1	↑	1	-	-	-	VC62P.5-0						(23h)
Description	- Adjust the gamma characteristics of the TFT panel. Positive Gamma Control '-': Don't care.												
Register availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

- NGC (E1h): Negative Gamma Control

E0H	Positive Gamma Control												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PGC	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)
1st parameter	1	↑	1	-	VC63N.3-0				VC0N.3-0				(F0h)
2nd parameter	1	↑	1	-	-	-	VC1N.5-0						(03h)
3rd parameter	1	↑	1	-	-	-	VC2N.5-0						(05h)
4th parameter	1	↑	1	-	-	-	-	VC4N.4-0					(09h)
5th parameter	1	↑	1	-	-	-	-	VC6N.4-0					(0Ch)
6th parameter	1	↑	1	-	-	VJ0N.2-0			VC13N.3-0				(0Fh)
7th parameter	1	↑	1	-	-	VC20N.6-0							(3Eh)
8th parameter	1	↑	1	-	-	VC36N.2-0			-	VC27N.2-0			(77h)
9th parameter	1	↑	1	-	-	VC43N.6-0							(4Fh)
10th parameter	1	↑	1	-	-	VJ1N.2-0			VC50N.3-0				(0Fh)
11th parameter	1	↑	1	-	-	-	-	VC57N.4-0					(17h)
12th parameter	1	↑	1	-	-	-	-	VC59N.4-0					(17h)
13th parameter	1	↑	1	-	-	-	VC61N.5-0						(21h)
14th parameter	1	↑	1	-	-	-	VC62N.5-0						(23h)

Description

- Adjust the gamma characteristics of the TFT panel.

Positive Gamma Control

'-': Don't care.

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value

		Power On Sequence	N/A	
		S/W Reset	N/A	
		H/W Reset	N/A	

- DTRCON (D9h): Dithering Control

D9H	Dithering Control												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PGC	0	↑	1	-	1	1	0	1	1	0	0	1	(D9h)
1st parameter	1	↑	1	-	EPF.1-0		EPFS	-	-	-	P24M.1-0		(00h)
2nd parameter	1	↑	1	-	CEPM.1-0		MG.1-0		MB.1-0		MR.1-0		(95h)

Description

-EPF.1-0: 16bit-to-18-bit pixel format conversion rule.

EPF.1-0	Description
"00"	R[0]=B[0]=0
"01"	R[0]=B[0]=1
"10"	R[0]=B[0]=MSB
"11"	R[0]=B[0]=G[0]

EPFS: EPF function selection for case EPF.1-0 = "11". This bit takes no effect when EPF.1-0 = "00", "01" and "10".

Setting this bit to '0' and EPF.1-0 = "11" -> R[0] = B[0] = G[0]. (Default setting)

Setting this bit to '1' and EPF.1-0 = "11" -> conditional copy for R[0] and B[0].

P24M.1-0: 24bpp color input mode. "00", truncation; "01", round; "1x" dithering. This parameter only take effect on 24bpp color input.

CEPM.1-0: Color enhancememt post-processing mode control: "00" truncation; "01": rounding; "10" dithering.

MR.1-0, MG.1-0, MB.1-0: Bayer matrix rotation for RED, GREEN, BLUE sub-pixel. 0: 0 degree; 1: 90 degree; 2: 180 degree; 3: 270 degree.

'-': Don't care.

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h/95h

		S/W Reset	00h/95h
		H/W Reset	00h/95h

- SRECON (DEh): SRE Control

DEH	SRE Control												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SRECON	0	↑	1	-	1	1	0	1	1	1	1	0	(DEh)
1st parameter	1	↑	1	-	DRK.5-0								(00h)
2nd parameter	1	↑	1	-	BRG.5-0								(00h)
Description	-DRK.5-0: Contrast gain control, ranged from -32 ~ +31, i.e -32/32 ~ +31/32 -> -1 ~ +0.96875. -BRG.5-0: A brightness offset added to an input pixel.ranged from -32 ~ +31, i.e -32/32 ~ +31/32 -> -1 ~ +0.96875. -Note that all 3 subpixels are added with the same value. '-': Don't care.												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

- RLCMODE (C8h): Run-length Control

<table>
<tr><td>C8H</td><td colspan="13">Run-length Control</td></tr>
<tr><td>Inst / Para</td><td>D/CX</td><td>WRX</td><td>RDX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>RLCMODE</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>(C8h)</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td>BDHM</td><td>PPBS</td><td>BLANKSEL</td><td>POLARITY</td><td colspan="2">BWSM.1-0</td><td colspan="2">CTRM.1-0</td><td>(0Ch)</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td></td><td></td><td></td><td colspan="6">RBNRTH.3-0</td><td>(08h)</td></tr>
<tr><td>3rd parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td></td><td></td><td></td><td colspan="6">GBNRTH.3-0</td><td>(08h)</td></tr>
<tr><td>4th parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td></td><td></td><td></td><td colspan="6">BBNRTH.3-0</td><td>(08h)</td></tr>
<tr><td>5th parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td colspan="7">RLC_EC.7-0</td><td>(00h)</td></tr>
<tr><td>Description</td><td colspan="13">-BDHM : Broken Display Handling Mode.
“0”: Display immediately black when write pointer catch up with scan pointer.
“1”: Display immediately black when write found.
-PPBS: Ping-pong buffer mode selected or not. It determine the operation mode for Run-length Codec FIFO memory.
“0”: A4KSRAM, which stacked by two 2K-byte SRAM blocks.
“1”: PING-PONG by two 2K-byte SRAM blocks.
-BLANKSEL: When write-over-scan or scan-over-write happen to FIFO, the decoded 1-bit pixel will be forced to the value specified by BLANKSEL.
When the FIFO has no meaningful encoded data in it, the decoded output also forced to the value specified by BLANKSEL.
“0”: Decoded 1-bit pixel forced to '0'.
“1”: Decoded 1-bit pixel forced to '1'.
-POLARITY: To determine if or not inverting the 1-bit pixel data, which binarized with RBNRTH.5-0, GBNRTH.5-0 and BBNRTH.5-0.
“0”: 1-bit pixel data after binarized will not be inverted.
“1”: 1-bit pixel data after binarized will be inverted.
-BWSM.1-0: Option to adjust the bit width of the codeword.
<table><tr><td>BWSM.1-0</td><td>Codeword Bit Width</td></tr><tr><td>00</td><td>5 bits</td></tr><tr><td>01</td><td>6 bits</td></tr><tr><td>10</td><td>7 bits</td></tr><tr><td>11</td><td>8 bits</td></tr></table>
-CTRM.1-0: Option for choosing the type of the code tree.
<table><tr><td>CTRM.1-0</td><td>Code Tree Types</td></tr><tr><td>00</td><td>weak white</td></tr><tr><td>01</td><td>balanced</td></tr><tr><td>1x</td><td>Only short-run</td></tr></table></td></tr>
</table>

-RBNRTH.5-0: Binarization threshold of Red-Color.

-GBNRTH.5-0: Binarization threshold of Green-Color.

-BBNRTH.5-0: Binarization threshold of Blue-Color.

-RLC_EC.7-0: To initiate spicific operation for RLC.

RLC_EC.7-0	Description
0xA5	To enable decoder test read function. Panel refresh operation will be stopped.
0x5A	To disable decoder test read function.

'-': Don't care.

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

- MIPIMODE (ECh): MIPI DPHY/DSI Control

ECH	MIPI DPHY/DSI Control												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PGC	0	↑	1	-	1	1	1	0	1	1	0	0	(ECh)
1st parameter	1	↑	1	-	F565	TXDIV2	ERPEN	EOTER_EN	ESCS_TREN	ESC_TREN	LPTX_TREN	HSRX_TREN	(F0h)
2nd parameter	1	↑	1	-	ESCS_TS.1-0		ESC_TS.1-0		LPTX_TS.1-0		HSRX_TS.1-0		(03h)
3rd parameter	1	↑	1	-	EOTPER_EN	TOFRX_EN	DSK0.1-0		CSK.1-0		RJTC_EN	RJTA_EN	(05h)
4th parameter	1	↑	1	-	TAGETM	-	TAGETS.5-0						(09h)
5th parameter	1	↑	1	-	TAGOM	-	TAGOS.5-0						(0Ch)
6th parameter	1	↑	1	-	-	-	ERST_EN	SETIM	ENPDN	V1_2SET.2-0(VCCLP)			(0Fh)
7th parameter	1	↑	1	-	-	SETI2.2-0			-	SETI1.2-0			(3Eh)

Description

-TXDIV2: To define ST7797 slave state TX period.

"0": TX state period 50nS.

"1": TX state period 100nS.

-ERPEN: MIPI Error Report enable bit. Default is disable.

- ERST_EN: To enable reset to MIPI DPHY/DSI by error found on MIPI BUS.

-HSRX_TREN: Enable HSRX Timeout function. '1': Enable; '0': Disable.

-LPTX_TREN: Enable LPTX Timeout function. '1': Enable; '0': Disable.

-ESC_TREN: Enable Escape Mode Timeout function. '1': Enable; '0': Disable.

-ESCS_TREN: Enable Escape Mode Silence Timeout function. '1': Enable; '0': Disable.

- EOTER_EN: Enabling "EOT" error detection. Default is off.

- TOFRX_EN: Forcing MIPI client circuit to be RX direction when HSRX timeout and LPTX timeout occurred.

- RJTA_EN: To enable "reject all packets after ECC 2-bit error found during HS".

- RJTC_EN: To enable "reject all driver commands except Cmd0x2C/3C during HS".

- TAGETM: Mode control for MIPI BTA TA-GET duration.

- TAGETS.4-0: Selection for MIPI BTA TA-GET duration control. Resolution is 100nsec/step. (TAGETS.5-0 + 1) x 100nsec.

- TAGOM: Mode control for MIPI BTA TA-GO duration.

- TAGOS.4-0: Selection for MIPI BTA TA-GO duration control. Resolution is 100nsec/step. (TAGOS.5-0 + 1) x 100nsec.

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes

		Partial Mode On, Idle Mode Off, Sleep Out	Yes
		Partial Mode On, Idle Mode On, Sleep Out	Yes
		Sleep In	Yes
Default			

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

14 REVISION HISTORY

Version	Date	Description
V1.0	2018/02	First Issue
V1.1	2018/07	Modify features